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Interfaces properties of low dielectric constant SiOC(-H) films deposited by plasma enhanced chemical vapor deposition

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The resistance capacitance (RC) delay in interconnects is increasingly becoming a limiting factor in overall circuit performance due to the continuous scaling of devices. The detailed electrical characterization of SiOC(-H)/*p*-Si(100) interfaces are studied with different progress parameters for ultra large scale integrated circuit (ULSI) multilevel interconnections. For the measurement of the SiOC(-H)/ *p*-Si(100) interfaces, the wafer has been cleaned in RCA solution and deionized water. And low dielectric constant SiOC(-H) films are deposited on *p*-type Si(100) substrates by plasma enhanced chemical vapor deposition (PECVD). Deposited SiOC(-H) films were annealed at the temperature from 250 ℃ to 450 ℃ in vacuum. Interfaces properties of SiOC(-H)/*p*-Si(100) with Al/SiOC(-H)/*p*-Si(100)/Al metal-insulator-semiconductor (MIS) structures have been investigated by capacitance-voltage (C-V) with flat band shift by electric field stress. Trapped charge, fixed charge and interface trapped charge of SiOC(-H)/*p*-Si(100) interface related to dielectric breakdown and leakage current density. Also, the dielectric breakdown induced microstructural changes in SiOC(-H) film are analyzed using high resolution transmission electron microscopy.