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Electrical characterization of $TiSi^2$ nanocrystals grown on multi-stacked tunnel layer for non-volatile memory

Seung Jong Han[1], Dong Uk Lee[1], Ki Bong Seo[1], Eun Kyu Kim[1]*, Jun-Seok Oh[2] and Won-Ju Cho[2]

[1]Department of Physics, Hanyang University
[2]Department of Electronic Materials Engineering, Kwangwoon University

The nano-floating gate memory (NFGM) based on nanocrystals (NCs) is a very attractive candidate for non-volatile memory application. The NFGM devices have a small operating voltage, long retention property, and fast program/erase speed. Despite these advantages, the NFGM devices have a problem of trade-off between program/erase efficiency and retention characteristics. Such problem can be improved using high-work function NCs and various tunneling layer.

In this study, we fabricated and characterized $TiSi_2$ nanocrystal non-volatile memory device with the barrier engineered tunnel layer. The $TiSi_2$ nanocrystal memory was fabricated on p-type Si (100) wafers. After cleaning wafers, the phosphorus in-situ doped poly-Si layer with a thickness of 100 nm was deposited on isolated active region to confine source and drain. And, the gate regions with the barrier engineered multi-stack tunnel layers were defined on Si substrates by using reactive ion etching. The 5-nm-thick $TiSi_2$ layer and the 30-nm-thick SiO_2 control layer were deposited on the multi-stacked tunnel layer by using magnetron sputtering. Then, the single layered $TiSi_2$ nanocrystals were created between the SiO_2 control layer and tunnel layer after post-thermal annealing at 800 ^{o}C for 2 min. The aluminum gate electrode of 200-nm-thickness was evaporated by using thermal evaporator. Finally, the photo-lithography and etching processes were carried out for defining of source-drain regions. The channel length and width of the transistor are the ranges of 2 - 10 μm. The electrical properties of devices were measured by using a HP-4156A semiconductor parameter analyzer. Also, the morphology of the $TiSi_2$ nanocrystals was analyzed by a transmission electron microscope.