Current equalization method of the rectifier diodes in LLC resonant converter Using the auxiliary winding of the transformer

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Abstract

The method for the current equalization of the rectifier diodes in LLC resonant converter is proposed. The method decreases the current difference between the rectifier diodes using the auxiliary winding of the transformer and asymmetrical pulse width modulation (APWM). The analytical reason of the current unbalance is investigated and the operation principle of the proposed method and APWM control loop are explained. The performance of the proposed method was verified on a 480-W, 400-V/24-V dc/dc converter.

1. Introduction

Recently, the role of the front-end dc/dc converter in SMPS of the consumer power electronics becomes more important because it affect to the system overall efficiency, reliability and cost. The limitations by pulse width modulation (PWM) converter such as efficiency decreasing at high frequency and high input voltage are well known. Therefore, the resonant converter starts to represent a high efficiency and high power density due to the soft switching. As the one of the attractive candidate topology for the front end converter, the LLC half bridge resonant converter is widely used in many applications such as flat TV, fuel cell, solar cell PCS, laser printer because it has several advantages such as: 1) the clamped switch voltage stress to the input voltage; 2) the soft switching achievement regardless of the load current; 3) simple circuitry through the utilization of the leakage inductance as a resonant device; 4) narrow switching frequency according to the load variation[1]-[2].

However, the current difference between the rectifier diodes is occurred especially in center-tapped rectification. The secondary side of the transformer for the center-tapped rectification requires dual winding. Due to the limitation of the mass product these winding, its leakage inductances and turns ratio are not identical. These mismatches between the secondary windings affect to the equivalent resonant tank and the resonant current. Therefore, it causes the unbalance of the power transmission and degrades the thermal distribution of the rectifier diodes. This phenomenon is especially serious in low output voltage, high current application. To overcome the problem, several methods have been proposed. The transformer winding technique to reduce the physical parameter mismatch between the secondary windings were reported.[3],[4] Nonetheless, the complex techniques decreases the productivity in mass production because it is manufactured by manual labor. The control method to compensate the current unbalance using the voltage across the rectifier diode is proposed. However, the controller for the compensation is implemented in secondary side.[5]

To realize the circuit in primary side, the current equalization method using the auxiliary winding voltage of the transformer is proposed. The auxiliary winding voltage contains the voltage across the magnetizing inductance. Thus, the virtual bias current information of the magnetizing inductance can be extracted from the winding voltage and it can be utilized with APWM.

In this paper, the analytical reason of the current mismatch is investigated. And then, the operation principle of the proposed method using auxiliary winding is explained. The performance of the proposed method is verified through the simulation result.

2. Current equalization of the rectifier diode in LLC resonant converter

2.1 The current mismatch phenomenon

The circuit diagram of the LLC half bridge resonant converter with center-tapped rectifier is shown in fig.1. In comparison with full bridge rectifier, the center-tapped rectifier gives less conduction loss and cost. Thus, it is mainly used in high current-low voltage application. In practical transformer, there exists the leakage inductance due to the secondary winding. These inductance values of the each winding W_1, W_2 are not identical because the each wire is wounded in different position respect to the primary side winding. The effect of the leakage inductance on secondary side to the voltage gain is researched in previous studies.[6] The equivalent resonant tank considering the secondary side leakage inductance is shown in fig.2. According to on and off of S_H switch, the conduction of D_H and D_L and reflected secondary side circuit is determined

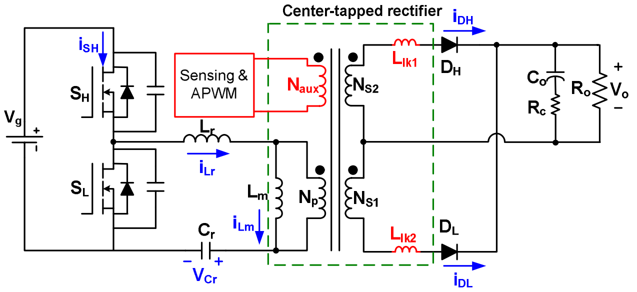

Fig. 1. The circuit diagram of the LLC half bridge resonant converter with center-tapped rectifier and proposed auxiliary winding.

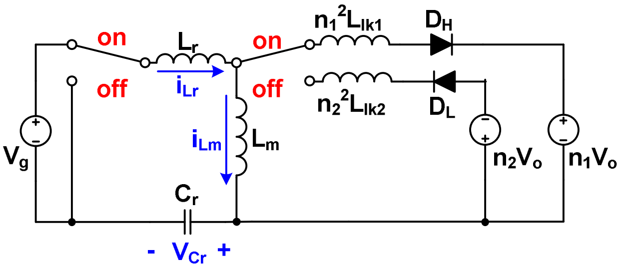

Fig. 2. The equivalent circuit of the resonant tank with center-tapped rectifier according to the on/off of S_H.

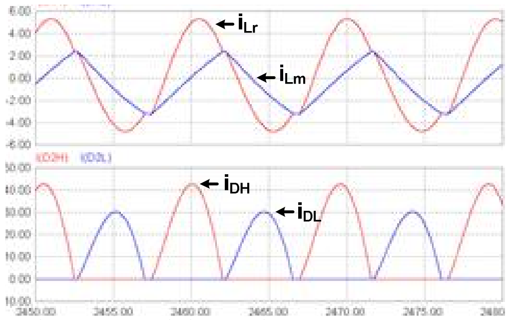

Fig. 3. The current unbalance when L_{lk1}=0.1uH, L_{lk2}=0.2uH and N_p:N_{S1}:N_{S2}=18:1.95:2.05

The turn ratios of the secondary side is normalized as n_1=(N_P/N_{S1}), n_2=(N_P/N_{S2}). The reflected secondary side leakage inductances are multiplied by square of normalized turn ratio. When S_H is turned on (defined as on period), D_H is conducted and the positive output voltage is reflected while D_L is conducted and the negative output voltage is reflected when S_H is turned off (defined as off period). Using the circuit analysis, relations of (1) can be obtained from the on period equivalent circuit in fig. 1.

$$V_g - L_r\frac{di_{Lr}(t)}{dt} - v_{cr}(t) = v_{Lm}(t) = L_m\frac{di_{Lm}(t)}{dt}$$

$$L_m\frac{di_{Lm}(t)}{dt} = L_{lk1}'\frac{di_{Llk1}'(t)}{dt} + n_1V_O \tag{1}$$

$$i_{Lr}(t) - i_{Lm}(t) = i_{Llk1}'(t), \quad C_r\frac{dv_{Cr}(t)}{dt} = i_{Lr}(t)$$

The resonant current during on period is obtained as (2)

$$i_{Lr\_on}(t) = i_{Lr01}\cos(\omega_{01}t) + \frac{V_g + v_{Cr01} - \left(\frac{n_1L_mV_O}{L_m + n_1^2L_{lk1}}\right)}{Z_{O1}}\sin(\omega_{01}t) \tag{2}$$

$$where,\ Z_{O1} = \sqrt{\frac{L_r + (n_1^2L_{lk1} // L_m)}{C_r}},\ \omega_{01} = \frac{1}{\sqrt{(Lr + n_1^2L_{lk1} // L_m)C_r}}$$

The resonant current during off period is acquired to (3)

$$i_{Lr\_off}(t) = i_{Lr02}\cos(\omega_{02}t) + \frac{v_{Cr02} + \left(\frac{n_2L_mV_O}{L_m + n_2^2L_{lk2}}\right)}{Z_{O2}}\sin(\omega_{02}t) \tag{3}$$

$$where,\ Z_{O2} = \sqrt{\frac{L_r + n_2^2L_{lk2} // L_m}{C_r}},\ \omega_{02} = \frac{1}{\sqrt{(L_r + n_2^2L_{lk2} // L_m)C_r}}$$

In ideal case, i_{Lr01} and i_{Lr02} from the (2) and (3) are same. v_{Cr01} and v_{Cr02} are equals to zero and V_g respectively. Thus, the term in the bracket highly affects. In case of high output voltage, the value of n_1 and n_2 are low. Thus, the effect of secondary side leakage inductance can be neglected due to the relation of (L_m>>$n^2{}_1L_{lk1}$) However, in low output voltage application, the effect of L_{lk1} and L_{lk2} are not neglected because n_1, n_2 becomes large. Unequal n_1, n_2 and L_{lk1}, L_{lk2} give rise to the different amplitude of each current resonant current and the unbalances are shown in fig.3. Since the power flow is concentrated on high side (S_H and D_H), the temperature of S_H and D_H is increased more than S_L and D_L. To reduce the effect of the different amplitude caused by un, the time duration of each mode should be controlled and this is key idea of the paper. To apply the idea to the practical circuit, sensing the error portion and the duty control method are required. Therefore, auxiliary winding voltage and asymmetrical pulse width modulation (APWM) are used in this paper. For the regulation of the output voltage, pulse frequency modulation (PFM) is used and APWM method should be operated giving the less effect to PFM operation. The sensing mechanism and operation principle of APWM will be explained detailed in 2.2.

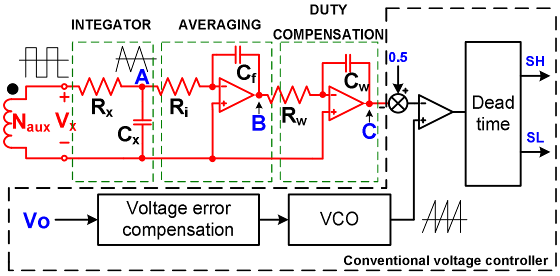

Fig. 4. The circuit diagram of the proposed method.

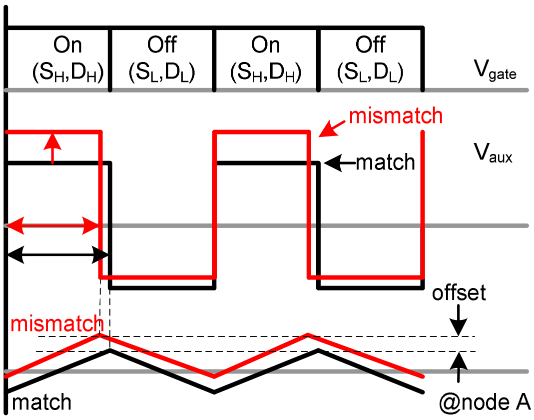

Fig. 5. The circuit diagram of the proposed method.

2.2 Current equalization by APWM using auxiliary winding

The detailed sensing circuit is described in fig.4. A single op-amp and R-C network are required to configure the sensing filter and duty compensation circuit. The voltage across L_m is induced to the auxiliary winding with turns ratio (n_{aux}=N_p/N_{aux}) and the voltage, v_{aux}, implies the information of the current difference. When all parameters of the transformer are same and the switches are driven by 50% duty ratio, V_{aux} is symmetrical shape like black line in fig. 5. The unequal parameters cause the different current from (2), (3) and it leads to unequal voltage magnitude across L_m in on and off period respectively. Thus, the time duration of on and off period also changed to satisfy the flux balance of L_m. In summary, the current errors of on and off period are transformed to the time differences. R_X-C_X integrator is connected to extract the time difference and presents as an offset voltage. Through the averaging of the waveform of node A, the error voltage (=offset voltage) which contains current difference information is generated at node B. The objective of the method is making the error voltage zero. In order to reduce the absolute value of the error, the duty compensation circuit is configured with zero reference. The output voltage in node C is added or subtracted from the default duty ratio 0.5. In order to minimize the interaction by duty compensation loop with respect to the voltage loop with PFM, the cut off frequencies of averaging filter and duty compensation are much less than the cut off frequency of the voltage loop gain. The low cut off frequency is reasonable because the unequal physical parameters are almost constant.

3. Simulation verification

For the performance verification of the proposed method, the circuit model is realized and simulated using PSIM software. The designed parameters and electrical conditions are listed in table I.

Table I. The circuit parameters and electrical conditions

Input voltage (V_g)	400V	Output capacitor(C_O)	9mF
Output voltage(V_O)	24V	Load current (I_O)	20A
# of N_{P1}	18T	# of N_{S1}	2T
# of N_{S2}	2T	# of N_{aux}	1T
Magnetizing inductance(L_m)	200uH	Resonant inductance(L_r)	35uH
Resonant capacitor(C_r)	33nF	Switching frequency (F_S)	85kHz~ 140kHz
R_X	10kΩ	C_X	10nF
R_i	100kΩ	C_f	47nF
T_i	0.001		

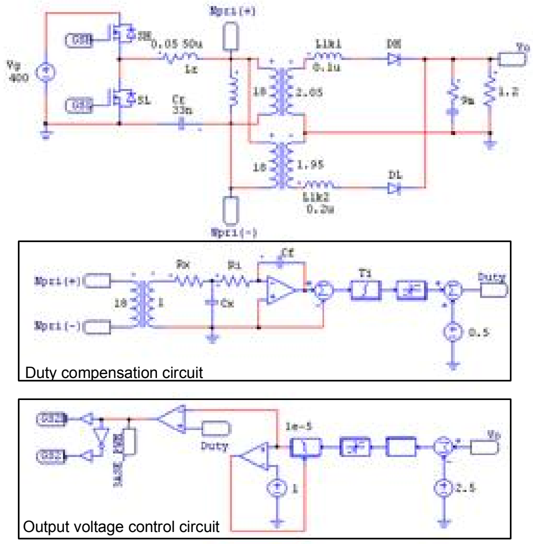

Fig. 6. The circuit diagram of the proposed method in PSIM

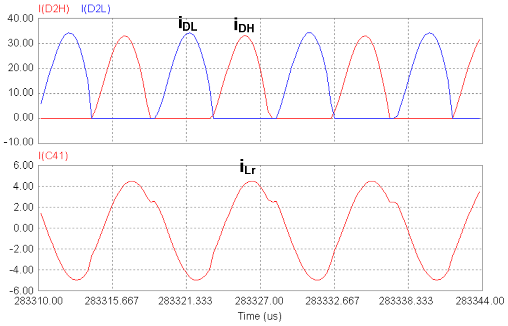

Fig. 7. The steady state waveform with proposed method

The circuit simulation is carried out using PSIM. The circuit diagram is shown in fig. 6. For the sensing the voltage across the magnetizing inductance, the auxiliary winding with filters are configured. The steady state waveforms are shown in fig.7. Before the compensation, the difference between the diode current is 10A in fig. 3. However, it is decreased to less than 1A with the proposed method. The duty ratios of high side and low side switches are changed to 0.53 and 0.47 respectively and the current shape of the resonant capacitor becomes asymmetrical. The transition waveform of the proposed method is shown in fig. 8. At initial, the current unbalance is observed. At 10ms, the proposed method is started and the current difference starts to decrease. The current waveform in bottom is resonant capacitor current. The offset current is also decreased to zero by the current balancing method. Since the gain of the integrator (T_i) can decrease the transition time, it generates the oscillation. Thus, 0.001 is selected in the simulation circuit.

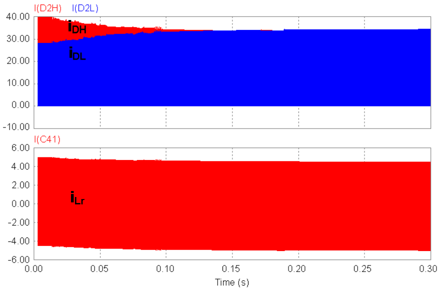

Fig. 8. The transition waveforms with the proposed method.

4. Conclusion

In this paper, the control method for the equalization of the unbalanced diode currents in LLC resonant converter is proposed. The main reason of the current unbalance is explained to find the way for the compensation. Using the auxiliary winding which includes the voltage across the magnetizing inductor, the asymmetrical duty ratio is determined and the current difference is decreased. The proposed method is implemented in primary side with low pass filters. The simulation results verify the performance of the proposed method.

Acknowledgment

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