1200V급 4H-SiC DMOSFET 성능지수 최적화 설계 시뮬레이션

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A simulation study on the figure of merit optimization of a 1200V 4H-SiC DMOSFET

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Abstract : In this work, we demonstrate 800V 4H-SiC power DMOSFETs with several structural alterations to observe static DC characteristics, such as a threshold voltage (V_{TH}) and a figure of merit ($V_B^2/R_{SP,ON}$). To optimize the static DC characteristics, we consider four design parameters; (a) the doping concentration (N_{CSL}) of current spreading layer (CSL) beneath the p-base region, (b) the thickness of p-base (t_{BASE}), (c) the doping concentration (N_J) and width (W_J) of a JFET region, (d) the doping concentration (N_{EPI}) and thickness (t_{EPI}) of epi-layer. Design parameters are optimized using 2D numerical simulations and the 4H-SiC DMOSFET structure results in high figure of merit ($V_B^2/R_{SP,ON}$>~340MW/cm^2) for a power MOSFET in V_B~1200V range.

Key Words : 4H-SiC, DMOSFET, current spreading layer, JFET

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