An IPD Based 2.5 GHz Power Divider for WiMax Applications

Ram Krishna Maharjan and Nam-Young Kim
RFIC Lab., Bima-Kwan.# 617-2, Department of Electronic Engineering, Kwangwoon University
447-1, Wolgye-Dong, Nowon-Gu, Seoul 139-701.

Abstract : This paper presents integrated passive device (IPD) based on Wilkinson power divider. The simulated 2-way power divider has the insertion loss of 3.123 dB, output isolation of -24.576 dB, input return loss of 26.415 dB, and output return loss of 33.478 dB. The power divider is based on IPD process design simulation at 2.5 GHz for WiMAX (Worldwide Interoperability for Microwave Access) applications. The chip size of power divider is 1 × 1.2 mm^2. which is under fabrication.

Key Words: Integrated passive device (IPD), MMIC, power divider, lumped elements, WiMax

1. Introduction

The IPD is an emerging technology. The microwave power splitters/combiners, such as Wilkinson power dividers are being commonly used, mainly in microstrip circuits. These power dividers are generally employed quarter-wave transmission line sections at the given frequency, which can have unrealistic dimensions at frequencies in the RF and low microwave bands, where the wavelength is large. Because of need of the daily use devices, all desire goods effective and smaller day by day, it would be preferable to use an equivalent power divider (i.e. based on IPD process) rather than microstrip and resistive type. Almost all type of microwave systems often need distributed RF power to various paths, for multiple applications. The easiest way to accomplish this is with power divider circuits. This type of power divider is also called 2-way(3dB) or three-port circuit.

2. Design and Simulation

The simulated power divider of 2.5 GHz frequency can be implemented in wireless communication system especially for the WiMax aplications. The lumped element type Wilkinson design based power divider will be fabricated on GaAs substrate separated integrated passive components by silicon nitrade(Si3N4) insulation. Nickel chromium(NiCr) thin film is used as a resistor. The cross-sectional view of GaAs substrate based IPD is shown in the Fig.1.

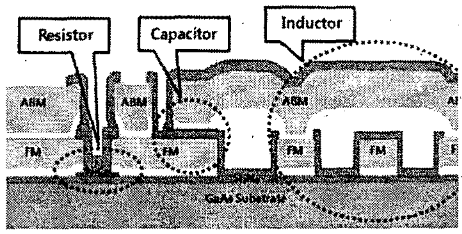

Fig.1 The cross-sectional view of IPD

Similarly the ADS based simulated circuit with foundry values is illustrated in the Fig.2. The chip size of power combiner is 1 x 1.2 mm^2.

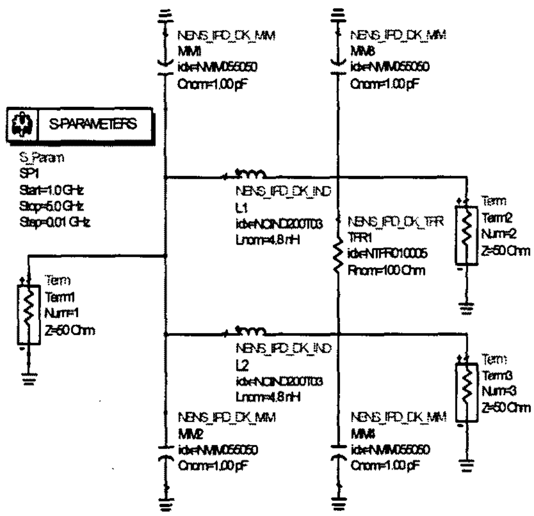

Fig.2 Three-port power divider

3. Simulation Results

In this paper, power divider is designed on the basis of Wilkinson power divider topology. It is under fabrication process of which cross-sectional view is shown in Fig.1. During simulation performance, values of L and C are optimized to achieve good simulation results. Resistor, R with 100 Ω is used to isolate the two input ports maintaining the input and output impedance of 50Ω (Fig. 2).

This circuit is a combination of two low pass filters separated by 100 Ω resistor. The power divider is based on GaAs IPD process at 2.5 GHz center frequency. The simulation results show the insertion loss(S21,S31) of 3.123 dB, the isolation between two output terminals(S23,S32) of -24.576 dB, the input return loss(S11) of 26.415 dB, and the output return loss(S22,S33) of 33.478 dB; which are illustrated in Fig.3. Design library is provided by NanoENS Company for this work.

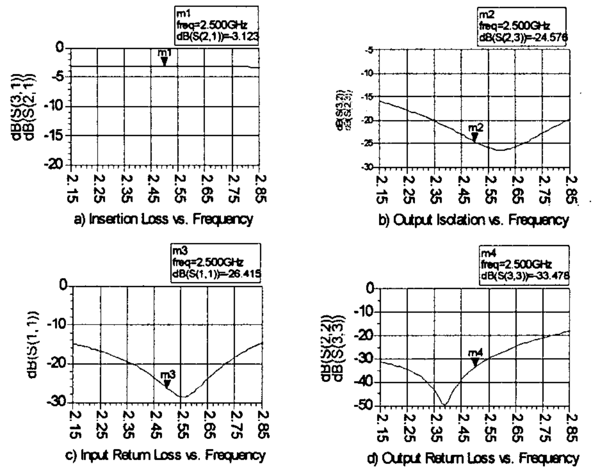

Fig.3 Insertion loss, isolation & return loss

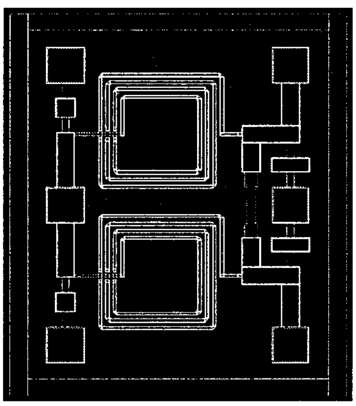

Fig.4 The layout design of 1 x 1.2 mm^2 chip area

The simulated power divider will be part of a wireless chip-to-chip interconnect system, as well as other wireless RF and microwave systems built on IPD based especially focused where needed limited space. The layout of the power divider based on simulated results which is under fabrication. The layout of the IPD power divider is shown in Fig.4.

4. Conclusion

This design work is based on IPD process power divider. The advantages of the design over the conventional power dividers or splitters are not only superior miniaturized compact size but also suppress output isolation response, and the lowest cost due to the mass product. Some of their applications include ratio measurements, balanced amplifiers, high-power transmitters, as well as antenna array feed networks.

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