IPD 기술을 이용한 Wilkinson 전력결합기 설계 및 전기장 시뮬레이션

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Compact Wilkinson Power Combiner Design and Electro Magnetic Simulation Using IPD Technology

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Abstract : In this paper, a power combiner using IPD process for SK Telecom 3-Generation (2.13 ~ 2.15 GHz) application. The Integrated Passive Device (IPD) Wilkinson power Combiner shows compact size and high performance. It is simulated by 3D Electro Magnetic (EM) simulation because of more accurate measurement result wire-bonding effects. This combiner exhibit size of 1.2mm^2 the insertion loss of 3.6 dB, and the return loss of 10.1 dB, and isolation of more than -7.7 dB.

Key Words : IPD, 3D EM simulation, Wilkinson Power Combiner

1. Introduction

Nowadays advanced modules for cellular phone applications continue to shrink in die size and cost. So small and easy to bring anywhere is a keen require and trend. This paper describes an Integrated Passive Device (IPD) process based on GaAs substrates design and EM simulation of high performance Wilkinson Power Combiner for application to SK Telecom 3-Generation (2..13 ~ 2.15 GHz) wireless communication system. In particular, we used CST simulator for simulating the device to obtain a precise EM result.

2. Integrated Passive Device (IPD) Process

Integrated Passive Device (IPD) technology based on Silicon wafer process has been in great interest in the past decade. This process is well familiar to the semiconductor industry. In the process, high density capacitors, high Q inductors, and large value resistors can be made. The component designs use finer width and spacing creating less parasitic effect, and this is the foundation from which smaller RF passive circuits [1]. Figure 1. shows a cross section of GaAs integrated passive devices. The fabricated substrate is a 6 inch SI-GaAs wafer with 0.625 mm thickness. GaAs substrate is able to high speed micro-electronics applications and shows a good permit of 12.85, and a loss tangent of 0.006. The process features two levels of plated Cu/Au metal. Frist metal with thicknesses of Cu 4.5 μm, and Au 0.5 μm, for the second metal with thicknesses of Cu 3.0 μm and Au 2.0 μm. The whole process starts with a bottom passivation layer which is composed of Si_3N_4 and deposited by PECVD(Plasma Enhanced Chemical Vapor Deposition) to thickness of 2,000 Å. Si_3N_4 used as the capacitor dielectric layer. Nicr metallization is used for thin film resistor thickness of 700 Å. Inductor is used air-bridge processing because more get high quality factor. All components are passivated with thickness of 3,000 Å Si_3N_4.

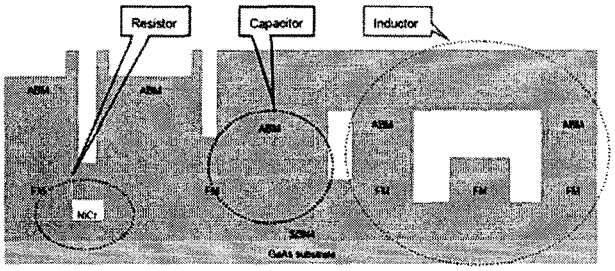


Fig.1. Cross section of GaAs IPD process .

3. Design of Wilkinson Power Combiner

Figure 2. shows a lumped-element version of a two-way power divider using π-equivalent low-pass LC networks. Typical lumped-element values for a power divider designed for 50 Ω impedance. This circuit also considered wire bonding effects. The isolation between the output ports is

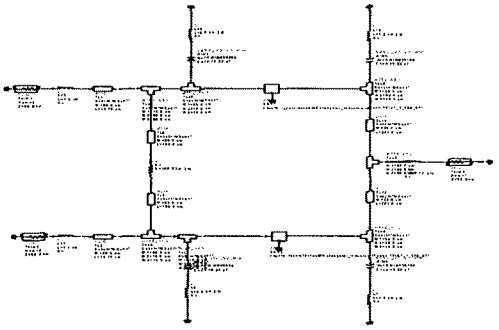


Fig.2. Three-port Wilkinson power combiner.

obtained by terminating the output ports by a series resistor R. Each of the quarter-wave lines has the characteristic impedance of $\sqrt{2}Z_0$, and the termination resistor has the value of $2Z_0$ Ω, with Z_0 being the system impedance. [2], [3]. Particularly, this circuit considered bonding-wire effect. So insert inductor factor is divided by bonding-wire length Figure 3. is final layout which is easy to bonding-wire and packaging.

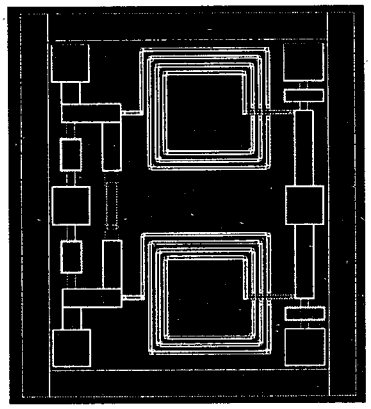


Fig.3. Layout design of 1 × 1.2 mm^2 chip area

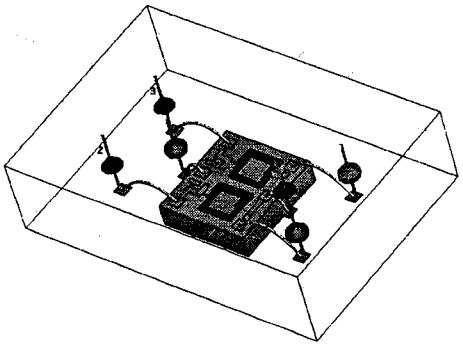
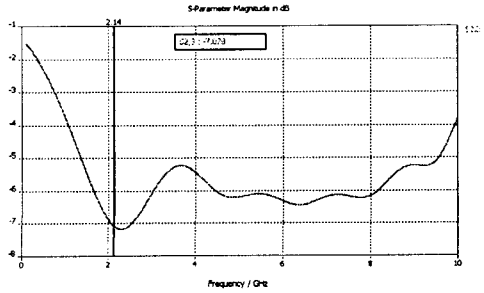


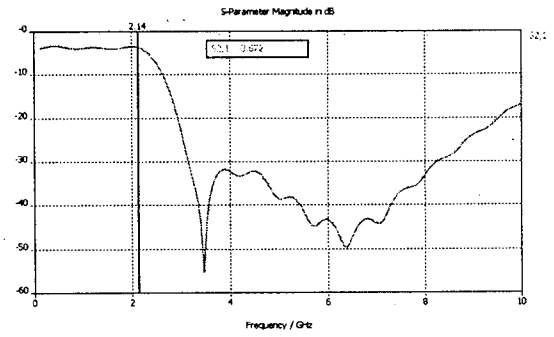
Fig.4. 3-D EM simulation of combiner and bonding-wire

4. Simulation Results

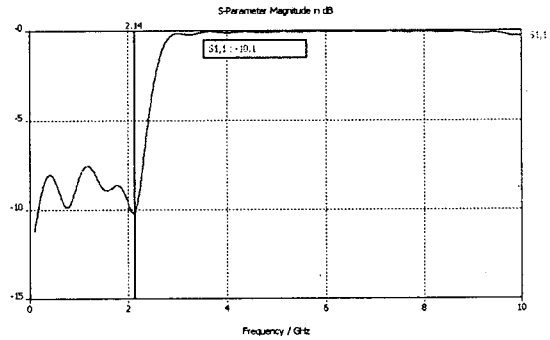
In this paper was used for EM simulation described. EM simulation is more accurately RF measurements of transmission lines, capacitors and inductor. Figure 5.. shows the comparison of simulated performance of power combiner. The EM simulation results show the insertion loss of 3.6 dB, the isolation between two port terminals of -7.7 dB, the input return loss of 10.1 dB output return loss of 6.2 dB



Isolation (S2,3)



Insertion loss (S2,1)



Return loss (S1,1)

Fig.5. Simulation result of EM simulation

5. Conclusion

IPD technology has been developed on GaAs substrate. EM simulations are extensively used in the development of this technology. EM simulation is more accurate expectation of measurement and best selection of layout design optimization all of components.

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