Fabrication of ZnO TFTs by micro-contact printing of silver ink electrodes

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Abstract

In this work, we have fabricated inverted staggered ZnO TFTs with 1-µm resolution channel length by micro contact printing (µ-CP) method. Patterning of micro scale source/drain electrodes without etching is successfully achieved by micro contact printing method by using silver ink and polydimethylsiloxane (PDMS) stamp. And the time dependent characteristics of the sheet resistance show that Ag inklayer could be used as source and drain electrodes for ZnO TFTs.

1. Introduction

Recently, ZnO thin film transistors (TFTs) have attracted much attention for their possible applications to flat, flexible, and transparent display devices such as active matrix liquid crystal displays (AM-LCD) and organic light emitting diode display (AM-OLED) panels than a-Si:H and poly-Si.[1-3] To realize low cost ZnO TFTs, it has been also emphasized to develop the printing technology. Toward the development of all-printed ZnO TFTs, a low resistance printed source/drain is crucial. Generally, the source/drain of ZnO TFTs is formed by vacuum deposition with shadow mask[2] and photolithographic pattering with etching equipment using etch stop layer[3], which are expensive and complex.

So, electrode patterns are manufactured by the high resolution direct printing techniques such as nano imprint (NIP) and micro contact printing (µ-CP). NIP can provide 70 nm resolution process but need etching process in high vacuum because of removing residual layer[5-6]. However, µ-CP method is the effective technique for direct micro patterning upto 100 nm without vacuum process. Therefore µ-CP method is the advanced candidate for simple and low cost patterning process without using complex vacuum system[7-10].

In this study, the source and drain electrodes having 1 µm gap width (which defines the ZnO TFTS channel length) were patterned by µ-CP method with Ag ink and polydimethylsiloxane (PDMS) stamp

2. Experimental

Figure 1 shows the process flow diagram of the fabrication for ZnO TFTs with Ag ink as source and drain electrodes in the case of top-contact (TC) configuration ZnO TFTs.

We prepared the silicon master using conventional photolithography method and etching process with 1.8 µm depth. The PDMS (Dow Corning Sylgard-184) stamp was fabricated using this master. The PDMS solution was thoroughly mixed 10:1 (Sylgard 184 A: Sylgard 184 B) and degassed in a desiccator for 30 minutes. Using vacuum pump, the poured PDMS on the Si master was degassed again to remove the trapped air bobbles, which were generated from the inside of the deep and narrow trench during the casting. For uniformity, the 1-mm-thick glass was adhered to PDMS solution in a µ-CP because PDMS mold had the flexibility. Ag ink was spin coated on the PDMS mold (3000 rpm, 30 sec). Then, the 300 Å thick ZnO active layer was deposited on SiO_2 (1000 Å)/Si substrate by Atomic Layer Deposition (ALD).

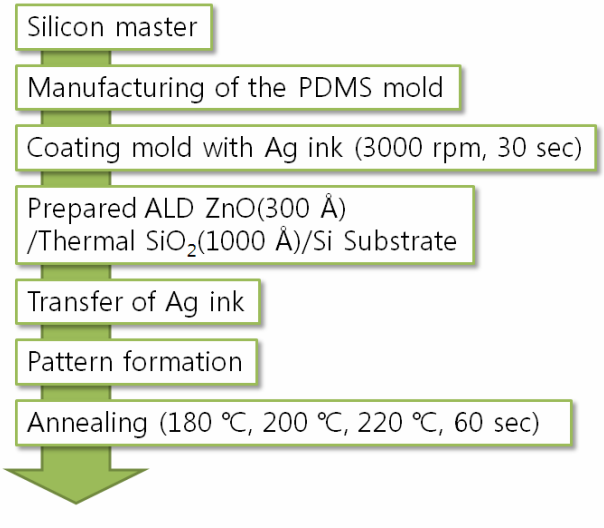

Fig. 1. Flow schematic diagram of our fabrication process for inverted staggered ZnO TFTs.

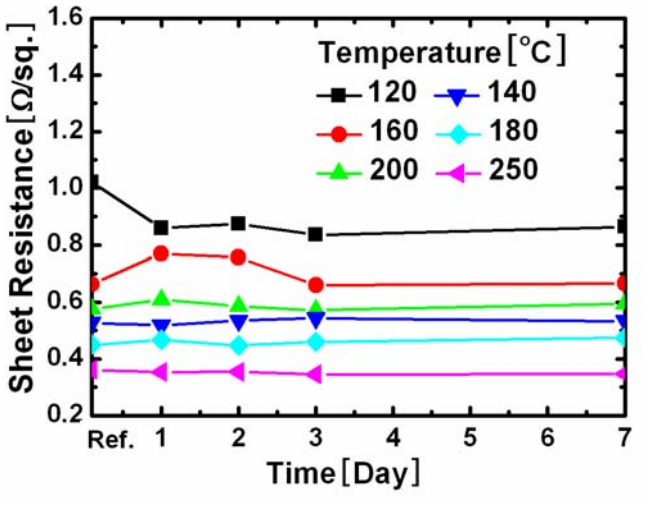

Fig. 2. Sheet resistance (R_{sh}) change of Ag ink layers as a function of annealing temperature and duration time in atmosphere condition.

The PDMS mold coated with Ag ink is put on the SiO_2/Si substrate Then, the PDMS mold was removed from the substrate, leaving the Ag source and drain pattern on pentacene layer. Finally, the Ag layer was baked on hotplate (180 °C, 200 °C, 220 °C, 60 sec) for dry solvent.

The current-voltage (I-V) characteristics of ZnO TFT was measured using HP 4156C Semiconductor Parameter Analyzer. Sheet resistance of Ag ink layer was measured using Four Point Probe System.

3. Results and discussion

Figure 2 shows the sheet resistance of Ag ink film layer as functions of annealing temperature and duration time in atmosphere condition. Annealing below 120 °C (not appeared in Fig.2.) , the sample has a high sheet resistance of 300 ohm/sq., but the sheet resistance abruptly decreased as the annealing temperature became 120 °C. In spite of the increase of duration time in atmosphere, the sheet resistance was maintained constant value. It is believed that Ag ink layer could be used as reliable source and drain electrodes of ZnO TFT.

Figure 3 shows the SEM image of the sample fabricated by μ-CP process. The length of source or drain pattern is about 1 μm. As the spin speed increased from 1000 to 4000 rpm, the thickness decreased from 2000 Å to 780 Å after annealing.

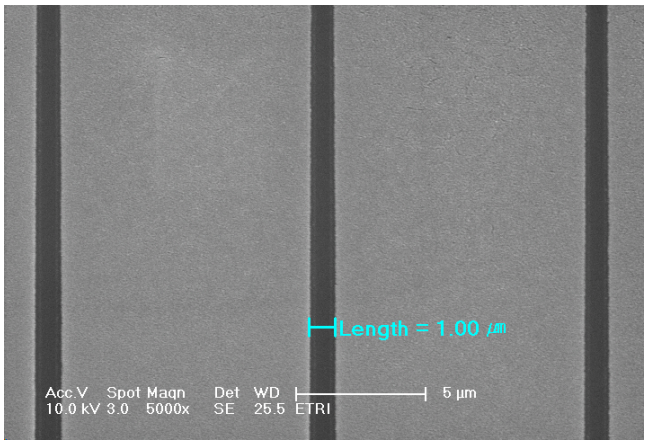

Fig. 3. FE-SEM images of the samples fabricated using μ-CP process. The length of source and drain electrode is about 1 μm.

Figure 4 shows the I-V characteristics of ZnO TFT with Ag source and drain electrodes. Figure 5 shows the total resistance change of ZnO with channel lengths of 1, 2, 3, 5, and 10 μm and channel width of 100 μm as a function of annealing temperature. The drain current and the on-off ratio were improved as the annealing temperature was increased. This result was highly related with the decrease of the contact resistance for the source or the drain under high annealing condition as shown in Fig. 5.

We investigated field effect mobility (μ), the threshold voltage (V_T), the sub-threshold slop (SS)

and the on-off ratio dependence on the annealing temperature. The results are summarized in Table I.

The field effect mobility and the on-off ratio were increase as the annealing temperature became higher. The field effect mobility (μ_{FE}) is 1.91 cm^2/Vs, the threshold voltage (V_T) is 1.51V, the sub-threshold slop (SS) is 1.05 V/dec. and the on-off ratio is 1.87×10^4.

4. Summary

Patterning methods with the photolithography and etching process or the shadow mask in vacuum progress were expensive and complex method. However, the proposed μ-CP method is the most possible process for the low cost, the low-temperature and the high resolution effective pattering for various electric applications. We made several PDMS mold from a master and fabricated μ-CP ZnO TFT for conductive Ag ink as an electrode material and ALD ZnO as a semiconductor on SiO_2. Although the samples were exposed in atmospheric conditions after annealing, there were negligible changes in sheet resistance. The drain current and the on-off ratio were improved as the annealing temperature was increased.

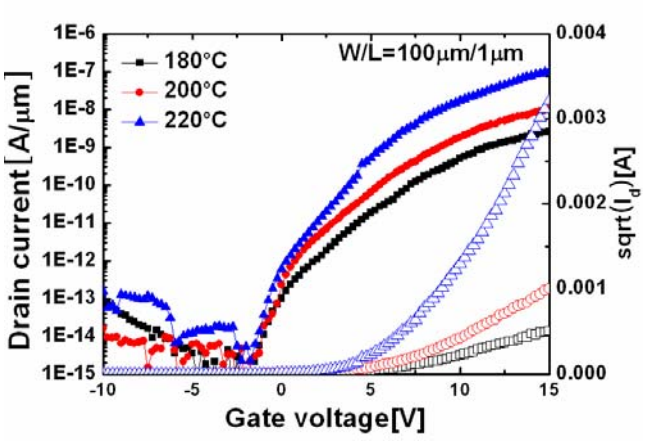

Fig. 4. Characteristic of a ZnO TFT fabricated using Ag source and drain electrodes (L=1 μm, W=100 μm). Drain current (I_D) vs. gate voltage (V_G) relation (Open : linear root I_D, Solid :Log I_D).

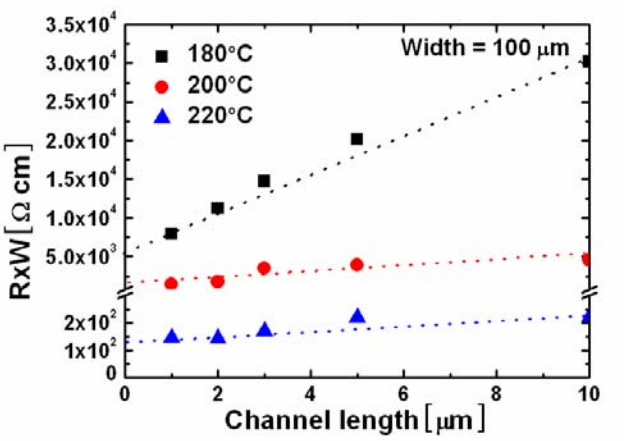

Fig. 5. Total resistance change of ZnO TFT with channel lengths of 1, 2, 3, 5, and 10 μm and channel width of 100 μm as a function of annealing temperature (@ Vg=15 V).

TABLE I. The electrical parameters of the ZnO TFT .

Annealing temperature[℃]	180	200	220
Mobility [cm^2/Vs]	**0.02**	**0.07**	**0.69**
Threshold voltage [V]	**4.78**	**4.81**	**4.88**
On-off ratio	**$7.03X10^6$**	**$2.79X10^7$**	**$4.56X10^7$**
Subthreshold Slope [V/Dec]	**0.82**	**0.84**	**0.63**

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