A Compact Cyclic DAC Architecture for Mobile Display Drivers

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Abstract

This work describes a power and area efficient switched-capacitor cyclic DAC for mobile display drivers. The proposed DAC can be simply implemented with one op-amp two capacitors and several switches. Furthermore, the op-amp input referred offset is attenuated at the DAC output without additional offset cancellation circuitry. The operation of the cyclic DAC is verified through circuit level simulations.

1. Introduction

Digital-to-Analog Converters (DACs) in column driver ICs for mobile display systems act the important part of data voltage generation [1-3]. The DACs for mobile displays are strictly required not only extremely low power consumption but also very compact chip implementation.

So far, 6-bit resistive DACs (RDACs) have been widely used for mobile display drivers including cellular phones, PDAs, and other wireless handsets [2], [3]. However, as the DAC resolution increases up to 8-bits and beyond to achieve finer gray scale, RDACs become extremely difficult to design due to the routing area involved with the resistor string, even though interpolative architectures are used. This leads to huge chip area as well as high power consumption. On the other hand, cyclic DACs (CDACs) using switched-capacitor (SC) circuits are good for small size low power mobile display drivers. A number of SC based CDACs have been proposed including [4] and [5]. However, [4] suffers from non-uniform switch channel charge injection, since the circuit configuration should change depending on the digital input data. In addition, the control clocking scheme for [5] is complicated, since it uses three capacitors.

In this paper, we propose an 8-bit SC CDAC using two capacitors. The circuit configuration does not change with the input data, which makes it robust to channel charge injection. In addition, the op-amp input offset is not critical. Overall, low power and small sized DACs can be obtained due to the simple control scheme.

2. Experimental

The proposed 8-bit CDAC generates the analog output from the digital input within 9-clock cycles, where 8-clocks are for the cyclic operation and 1-clock is for the capacitor reset. Each cyclic operation includes 2-phases (phase-1 and phase-2). The LSB of the digital data is first applied to the CDAC.

Fig.1 shows the SC circuit configuration of the proposed CDAC for phase-1 and phase-2, respectively. The value of feedback capacitor (2*C*) is twice of the sampling capacitor (*C*). In addition, the circuit is identical for each phase regardless of the value of the input data. Assuming 8-cycles are required for the CDAC to generate the final output, the *i*-th cycle CDAC output is given as

$$V_o(i) = V_{REF} \cdot \left[\frac{b_{i-1}}{2} + \sum_{k=0}^{i-2} \frac{b_k}{2^{i-k}} \right] \quad (i \geq 2) \qquad (1)$$

where V_{REF} is the reference voltage and *b* is digital input bit that is either 1 or 0. As shown in Eq. (1), the output consists of the incoming bit (first term) and the residue (second term). This describes the operation of the CDAC where the incoming data and the residue are all halved before scaled by V_{RFE}.

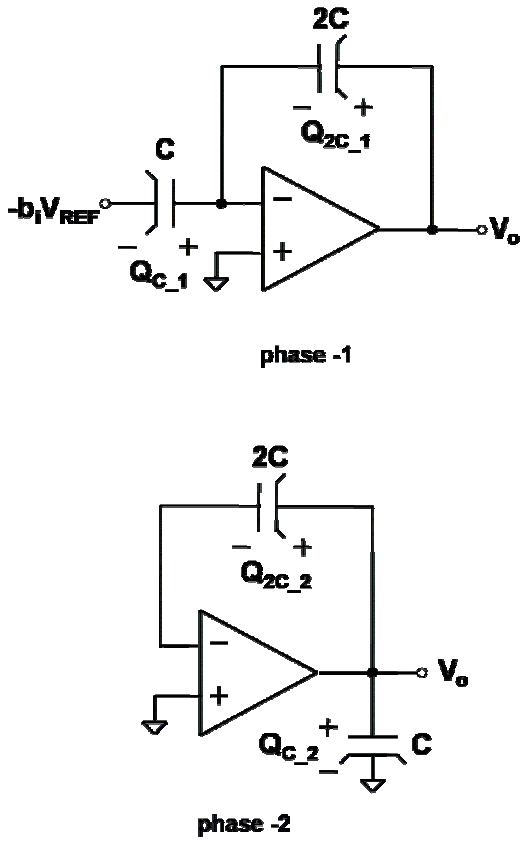

Fig. 1. Circuit configuration of the proposed CDAC.

During phase-1, the incoming bit is sampled in C, and the residue is stored in $2C$. The incoming bit and residue corresponds to the first and second term of Eq. (1), respectively. In phase-2, the residue stored in $2C$ is copied to C, however the value is halved due to the capacitor ratio (2:1). As a result, in the next phase-1, half of the residue will be stored in C along with the incoming bit, which will be subtracted from the residue stored in $2C$. This will scale the residue by 1/2. In addition, for each phase, the CDAC output will be halved once more due to the 2 to 1 capacitor ratio, which will eventually lead to Eq. (1).

The charge equation for each phase can be obtained as follows. At the beginning of phase-1, the charge stored in C and $2C$ for the i-th cycle are given as

$$Q_{C\_1}(i) = C \cdot V_o(i-1) \tag{2a}$$

$$Q_{2C\_1}(i) = 2C \cdot V_o(i-1) \tag{2b}$$

where $V_o(i\text{-}1)$ is the CDAC output for (i-1)-th cycle. As shown in Fig. 1, the residue charge remains in $2C$, and half of this charge is stored in C, which is the same charge for the previous phase-2. In addition, at the end of phase-1, the charge remaining in C and $2C$ for the i-th cycle are given as

$$Q'_{C\_1}(i) = C \cdot V_{REF} \cdot b_{i-1} \tag{3a}$$

$$Q'_{2C\_1}(i) = C \cdot V_{REF} \cdot b_{i-1} + C \cdot V_o(i-1) \tag{3b}$$

where $b_{i\text{-}1}$ is the incoming bit which is either 1 or 0. Now, the charge corresponding to the incoming bit is stored in C, and the same amount is mirrored in $2C$. In addition, the residue charge stored in C is transferred to $2C$, and it is subtracted from the previous residue charge stored in $2C$. That is, the second term of Eq. (2a) is subtracted from the second term of Eq. (2b). As a result, the remaining charge will be the second term of Eq. (3b).

The charge stored in $2C$ at the end of phase-1 remains the same in phase-2. Therefore, the residue charge in $2C$ for phase-2 (i-th cycle) can be written as

$$Q_{2C\_2}(i) = Q'_{2C\_1}(i). \tag{4}$$

In addition, the charge stored in C for the i-th cycle can be obtained by

$$Q_{C\_2}(i) = C \cdot V_o(i) \tag{5}$$

where $V_o(i)$ is the CDAC output for the i-th cycle. The charge induced in C is obtained by sampling the CDAC output voltage that is generated from the residue charge stored in $2C$. However, charge stored in C will be halved due to the capacitor ratio. Therefore, Eq. (5) can be rewritten as

$$Q_{C\_2}(i) = 0.5 \cdot Q_{2C\_2}(i). \tag{6}$$

Output of the proposed CDAC remains the same for both phase-1 and phase-2, since the residue charge stored in $2C$ does not change once the charge for the incoming bit is mirrored, and the residue charge subtraction is completed during phase-1. The CDAC output for the i-th cycle can be obtained by

$$V_o(i) = \frac{Q'_{2C\_2}(i)}{2C} \tag{7}$$

where the $V_o(i)$ leads to Eq. (1). The final output of the 8-bit CDAC after 8-cycles of repeating phase-1 and

phase-2 is given as

$$V_o = V_{REF} \cdot \sum_{i=0}^{N-1} \frac{b_i}{2^{N-i}} \quad (8)$$

where N =8, and b_i is the i-th input bit.

The input referred offset of the op-amp will have a similar behavior as the digital input bits. During phase-1, the offset will be sampled in C, and the same offset charge will be mirrored in $2C$. In phase-2, the charge stored in $2C$ will remain constant whereas half of the offset charge will be sampled in C that will be subtracted from the residue offset charge in $2C$ during the next phase-1. Therefore, after 8 cycles, the offset voltage at the output of the CDAC is given by

$$V_{o,offset} = V_{os} \cdot \sum_{i=0}^{N-1} \frac{b_i}{2^{N-i}} \quad (9)$$

where V_{os} is the op-amp input offset, and N = 8. It is shown that $V_{o,offset}$ is always less than V_{os}.

3. Results and discussion

The complete circuit and operation timing of the proposed CDAC is shown in Fig. 2. The operation includes 8-cycles of conversion and 1-cycle of reset where, the final output is valid during the 8th cycle. The switches controlled by R and R_B are for reset. A conventional non-overlapping 2-phase clock is used for each cycle to put the circuit in phase-1 and phase-2 configuration.

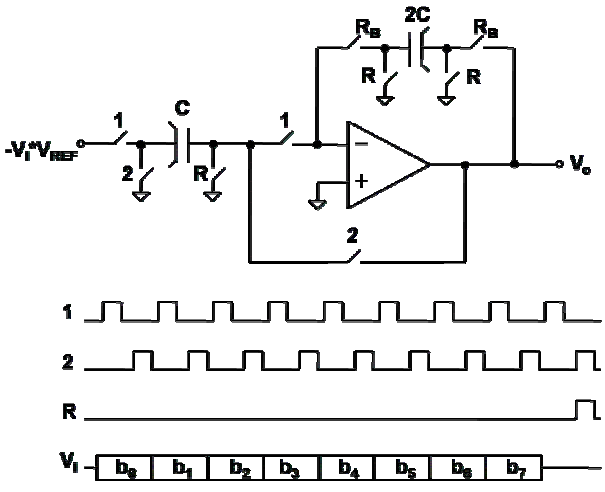

Fig. 2. Complete circuit and timing of the CDAC.

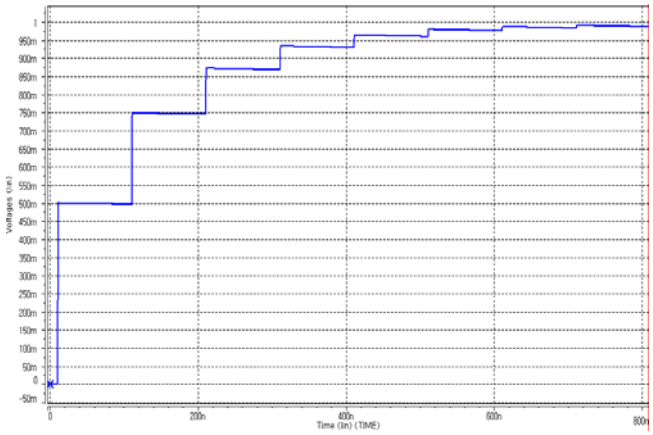

Fig. 3. CDAC output waveform to the input value of 11111111.

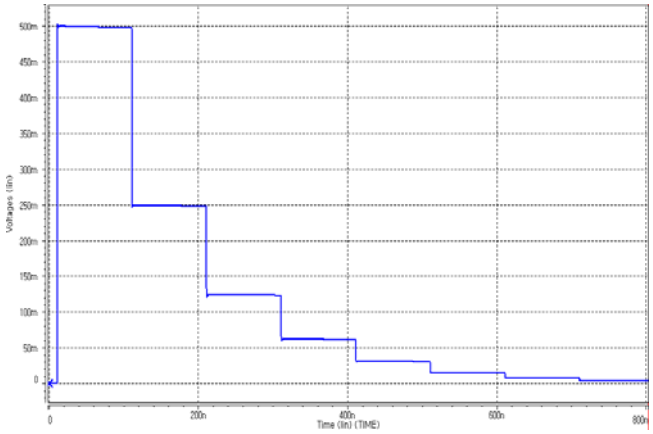

Fig. 4. CDAC output waveform to the input value of 10000000.

For both capacitors C and $2C$, the top plates are always connected to the input summing node of the op-amp, which reduces the parasitic effect. In addition, since the SC configuration of the CDAC does not change with the input data, the channel charge injection will be constant regardless of the input value. This will minimize the data dependent non-uniform channel charge injection, which degrades the INL of the CDAC.

The circuit level CDAC was simulated with *hspice*. Fig. 3 shows the output waveform with digital input = 11111111. It is shown that the output is changing for each clock cycle, and approaching the final value 996.09375mV. Fig. 4 is the output waveform with digital input = 10000000. In this case, the first cycle output is 500mV, and the final value is 3.90625mV which is the V_{LSB} of the CDAC.

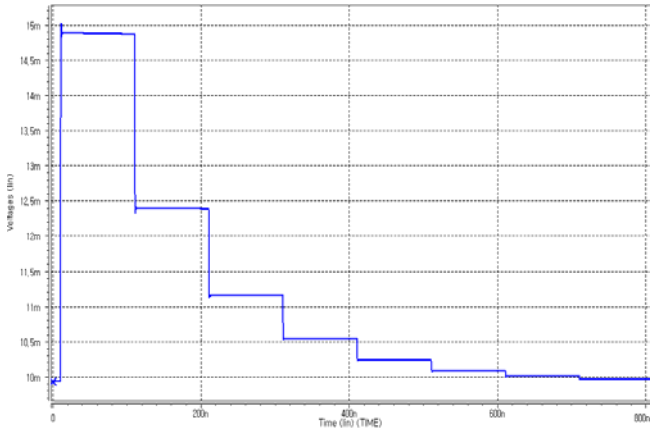

Fig. 5. CDAC output waveform with op-amp input offset = 10mV and input = 00000000.

Fig. 5 is the CDAC output waveform with op-amp input offset of 10mV. For this case, the digital input bits were all set to 0, in order to clear see the effect of the offset. As shown in Fig. 5, after 8-clock cycles, the final output of the CDAC is slightly less than the original offset which is 10mV. This can be explained by the analysis result described in Eq. (9). As a result, the op-amp input offset is attenuated at the output of the CDAC.

Overall, the operation of the proposed CDAC using different digital input patterns, and the effect of op-amp offset is verified through circuit level simulations.

4. Summary

In this work, a power and area efficient 8-bit SC CDAC is presented. The proposed CDAC can be implemented using one op-amp and two capacitors with a simple switch clocking scheme. The circuit configuration does not change with the input data, which makes it robust to channel charge injection. Furthermore, the op-amp input offset does not degrade the performance. As a result, the proposed CDAC can be a good solution for low-power and small-size mobile display drivers.

Acknowledgement

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5. References

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