Residual stress on nanocrystalline silicon thin films deposited with substrate biasing at low temperature

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Abstract

Nanocrystalline silicon thin films were deposited using an internal-type inductively coupled plasma-chemical vapor deposition at room temperature by varying the bias power to the substrate and the structural characteristics of the deposited thin film were investigated. The result showed that the crystalline volume fraction was decreased with the increase of bias power. At the low bias power range of 0~60 W, the compress stress in the deposited thin film was in the range of -34 ~ -77 Mpa which is generally lower than the residual stress observed for the nanocrystalline silicon thin films deposited by capacitively coupled plasma.

1. Introduction

Nano/microcrystalline silicon thin films are widely used in electronic and optical devices, such as thin film transistors (TFT), solar cell, image sensors, etc. [1]. In fact, nano/microcrystalline silicon can be directly deposited with CCP-PECVD without annealing by using highly diluted SiH_4 gas mixtures and at a high substrate temperature. However, the deposition rate is very low and, due to a high plasma potential, the silicon deposited can be easily damaged. Inductively coupled plasma (ICP) which has a relatively high plasma density ($>10^{11}/cm^3$) [2, 3] and a low plasma potential [4] can be used in the deposition of nano/microcrystalline silicon at a higher deposition rate and at a low temperature. Among the various ICP sources, the internal-type ICP is known to be more applicable to extremely large area substrate such as TFT-LCD, therefore, its plasma characteristics were extensively investigated by previous studies [4-5].

In this study, the ion energy to the substrate was varied by applying RF bias power to the substrate and the effect of bias power to the structural properties of the deposited nano-, microcrystalline silicon thin film was investigated for the understanding of the damage by ion bombardment during the deposition of silicon thin film.

2. Experimental

A schematic diagram of the ICP-CVD system used in this experiment is shown in Fig. 1. Double comb-type ICP source was installed in a rectangular chamber having the inner size of 1,020 mm x 830 mm. To deposit silicon thin films, Corning 1737 glass and single-crystal silicon wafer were used and, during the deposition at RT, the substrate was biased by a separate 12.56 Mhz rf power supply and the bias power was varied from 0 to 240 W during the deposition. The rf power was fixed at 4 kW, while the SiH_4 concentration, total gas flow rate, and working pressure were maintained at 10 %, 200 sccm, and 20 mtorr, respectively.

The crystallinity of the deposited nano-, microcrystalline silicon thin film was investigated by using micro-Raman spectroscopy. A residual stress measurement tool was used for the determination of the residual tensile or compressive stress in the films by measuring the changes of the substrate curvature using the Stoney’s equation before and after the deposition at room temperature [6-7].

3. Results and discussion

Fig. 2 shows the Raman spectra of the nano-, microcrystalline silicon thin film deposited as a function of RF bias power. From the Raman spectra, not only the crystallization percentage of the thin film but also the amount of residual stress in the film can be calculated by the shift of main peak position from that of crystal silicon (520 cm^{-1}). As shown in the figure, the Raman peak positions of the deposited nano-, microcrystalline thin film were close to 520 cm^{-1} showing the formation of crystalline silicon thin film. Also, as shown in the figure, the intensity of the Raman peak was slightly decreased with the increase of RF bias power indicating the decrease of crystallinity with the increase of bias power.

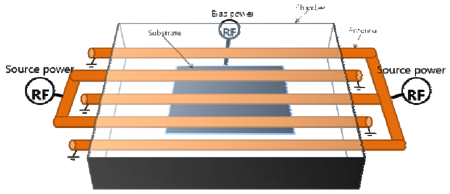

Fig. 1. Schematic diagram of the double comb-type internal ICP.

Also, the shift of Raman peak to longer wave number (redshift) with the increase of RF bias power showed the increase of residual stress in the film.

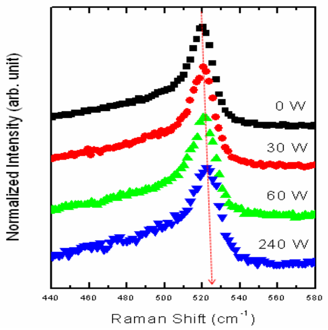

Fig. 2. Raman spectra of silicon thin films deposited as a function of various substrate RF bias power[8].

The calculated residual stress is shown in Fig. 3 as a function of RF bias power and the residual stress was increased from -34.43 MPa at no RF bias power to -594.3 MPa at 240 W of RF bias power almost similar to the residual stress estimated by the Raman spectral peak shift.

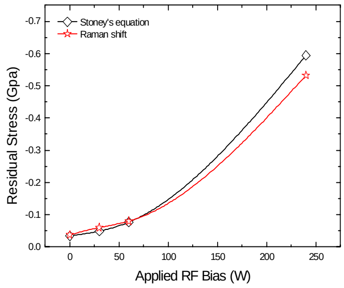

Fig. 3. The residual stress measured by a residual stress measurement tool using Stoney's equation and the residual stress estimated by Raman spectral red shift are shown[8].

Compared with the results by V. Paillard et al., the residual stress obtained in our experiment by internal-type ICP-CVD at low RF bias powers (0~ 60 W) is significantly lower than those obtained by CCP-CVD. The lower residual stress obtained in our experiment even with a RF bias power is believed to be related to the lower plasma potential obtained in the ICP-CVD system.

4. Summary

The structural properties of the deposited thin film such as crystalline volume fraction and residual stress were investigated to study the degree of physical damage by ion bombardment. The increase of RF bias power decreased the crystallization volume fraction and increased the residual compress stress in the deposited thin film. The decrease of crystalline volume fraction and the increase of the residual compress stress with the increase of RF bias power are related to the damage to the substrate by the increased ion bombardment energy. However, possibly due to the low plasma potential, which causes the lower ion bombardment energy, the residual stress measured at low RF bias power conditions in the experiment was generally lower than those of crystalline silicon thin film obtained by CCP-CVD without RF biasing.

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5. References

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