Thin Film Transistor fabricated with CIS semiconductor nanoparticle

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Abstract

Thin Film Transistor(TFT) having CIS (CuInSe) semiconductor layer was fabricated and characterized. Heavily doped Si was used as a common gate electrode and PECVD Silicon nitride (SiN_x) was used as a gate dielectric material for the TFT. Source and drain electrodes were deposited on the SiN_x layer and CIS layer was formed by a direct patterning method between source and drain electrodes. Nanoparticle of CIS material was used as the ink of the direct patterning method

1. Introduction

Recently, tremendous developmental demands for printed electronics are widely experienced. For example, RFIDs are being developed in a platform of the printed electronics. Typically, the platform is frequently on the basis of organic material to constitute electronic devices [1]. However, the electrical performance of the organic material-based device is still far behind of that of inorganic material-based device. Instead of organic material, very recently, silver ink is intensively introduced for device fabrication of printing electronics [2]. In this study, CIS nanoparticle was used as a printing ink of semiconductor layer for fabrication of thin film transistor. The CIS semiconductor ink was applied by a simple dropping or a direct patterning method, such as piezo inkjet. Output and transfer characteristics of CIS TFT were characterized.

2. Experimental

For CIS(CuInSe) semiconductor thin film transistor (TFTs) fabrication, a heavily boron (p+) doped silicon substrate was served as the gate in an inverted-gate structure. For dielectric layer, SiN_x films, grown by PECVD(RF-frequency HF 13.56MHz, LH 400KHz) at 400℃ was used. The deposition pressure was 0.3mTorr and resultant film's refractive index was 2.02. After deposition of the dielectric layer, 100 nm thick aluminum layers were evaporated with source and drain patterned shadow mask on top of the SiN_x substrate. Two aluminum electrodes (source–drain) with a channel width–to-length ratio of 2 (channel length equals 200 μm) were formed on the SiN_x layer. After the CIS semiconductor was formed by a direct patterning method between source and drain electrodes, the films were annealing at 400 ◦C for 1 h in an N_2 atmosphere. Finally, a schematic cross-sectional view and microscopic photograph of the fabricated transistors are depicted in Fig. 1. I–V curves were obtained for the fabricated field-effect TFTs with an Agilent 4145B semiconductor parameter analyzer in ambient condition.

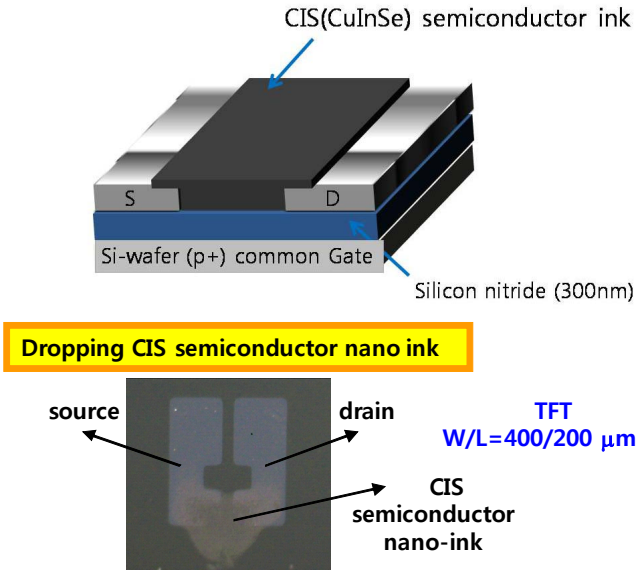

Figure 1. Schematic diagram ad microscopic photograph of fabricated TFTs silicon substrate.

3. Results and discussion

The field-effect characteristics of the TFTs fabricated on silicon substrates were investigated. Figure 2 shows the plot of I_D versus V_D modulated by applying a gate voltage ranging from 0 to -20 V for a representative TFT fabricated on a silicon substrate. It shows a typical characteristic of a p-channel transistor with a saturation region. The ON/OFF current ratio (I_{ON}/I_{OFF}) was about 10^2. Although the large ON current level is achieved, a high OFF-current level in the sub-micro ampere range results in a small (I_{ON}/I_{OFF}) ratio compared with conventional silicon-based TFTs. It is reported that the operating gate voltage can be reduced by substituting thin Al_2O_3 for thick SiO_2 bottom gate dielectric that is used in most solution-processed inorganic transistors [3]–[4]. Therefore, the SiN_x layer in our experiment can be substituted for more optimized device performance.
In this study, by introduction of a new material of CIS nanoparticle for active layer of TFT, a high performance device can be made with direct-patterning method technology. It can be a breakthrough technology to make a real mass production of printed electronics, such as flexible display

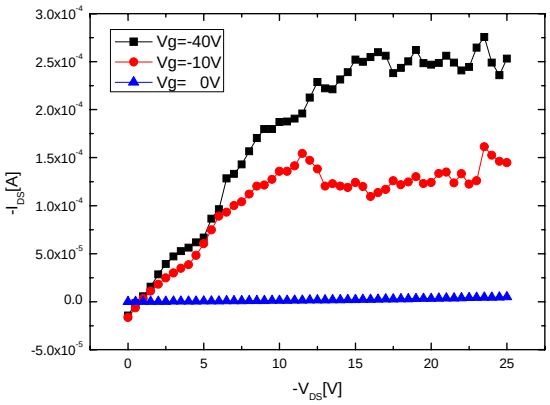

Figure 2. Output characteristics of a CIS (CuInSe) nanoparticle TFT.

4. Summary

TFT having CIS (CuInSe) semiconductor layer fabricated by dropping CIS nanoparticle ink was characterized. The TFT showed a high current level of output characteristic and low ON/OFF current ratio of 10^2. Provided the low I_{ON}/I_{OFF} is improved, CIS nanoparticle TFTs have the potential to be used as the building blocks for a high performance TFT device.

5. References

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