LCD Cell Aging Tester

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Abstract

This paper suggests that testing method and equipment structure to detect potential failures of LCD cells. LCD Cell Aging Tester is the unique process to detect failures related with ASG circuits. This system consists of four components that is Aging chamber, work table, probe contact unit, and pattern generator. The key factor of the concept is temperature aging and HVS driving. Complicated combination of test parameters including voltage, temperature and frequency provided practical burn-in conditions eligible for prediction of mass production.

1. Introduction

Recently, there are growing demands for flat panel display (FPD) devices to be lower-priced, lower-electricity consuming, and more productive. TFT LCD business is largely growing with its rapid development[1] in performance and productivity most of all FPDs. And besides, LCD is the most appropriate technology for system on a glass (SOG)[2, 3] solution. LCD Module manufacturing is now classified as a low-value-added business with lowered entrance barrier to its market and its generalized technology. In this circumstance, LCD manufactures are focusing on development and research for panel manufacturing stage, enabling mass production at higher volume applied with competitively developing technologies for SOG, faster motion picture response time and quicker transmissivity. Accordingly, the demands for higher reliabilities of LCD are much growing and it will be beneficial to introduce a stress test to detect potential failure of LCD cells in advance. In this paper, we suggest the introduction of a new testing concept and its process, including Aging condition[4,5,6], probe contact unit, high voltage stress (HVS)[7], and driving condition of pattern generator to detect the failures of amorphous silicon gate (ASG)[8,9] circuit.

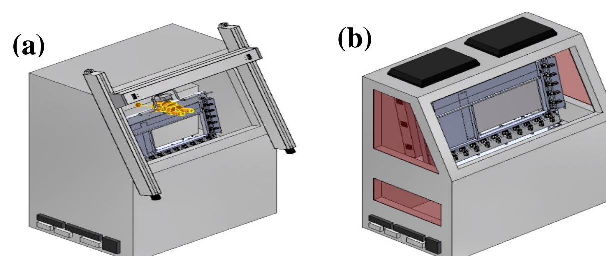

Fig. 1. Demo version of Cell Aging Tester (a)Test site for standard feature (b)Test site combined with Aging chamber.

2. Experimental

ASG circuit is composed of transistors (TR) that are functioning as GATE driver ICs. If one of them is to be broken, then related line including broken TR will be in failure [8, 9].

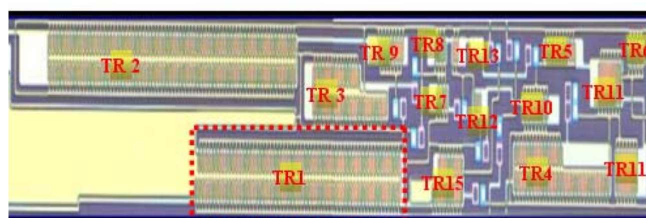

Fig. 2. Lay-out of ASG circuit composed by TRs which functioning as GATE Driver IC.

Stress test was conducted by aging condition controlling and HVS driving with three methods of probe contact in combination. Aging chamber

detecting potential failures for ASG circuit was newly developed. Testing objectives was half-finished panels with built-in ASG circuits. Many cases of contact method applying driving signal to TFT devices have been reported. We adopted three methods with (for those of) probe pin contact unit to pads of cell : 1) Full line contact for auto probing[10], 2) Shorting bar pads contact[11], and 3) 1G1D bundle contact[12,13]. Driving signal was applied during HVS aging. Detailed conditions for voltage and frequency were as follows, which are summarized in Table 1 .

- GATE voltage applied from -15V to +35V, as 0.1V unit controllable.
- DATA voltage applied from -10V to +10V, as 0.1V unit controllable.
- Vertical Frequency applied from 30.0Hz to 110Hz, as 0.1Hz unit controllable.

Also Temperature aging test was conducted in condition from Room Temp. to 65° C, as 1° C controllable.

TABLE 1. Condition of HVS driving.

	GATE	DATA	Common	Frequency
Normal	+25V	±5V	+5V	60 Hz
Upper	+35V	+10V	+10 V	110 Hz
Lower	-15V	-10V	- 5 V	30 Hz

3. Results and discussion

Fig. 3. shows the microscope images of display panel during turn-on operation. Under normal condition, no obvious failure was detected while ASG failure after HVS aging at 60° C for two hours was observed to be black line. HVS was done at appropriate condition within the window shown in Table 1. It was found that potential failures related to ASG circuit were dependent upon aging and drive condition.

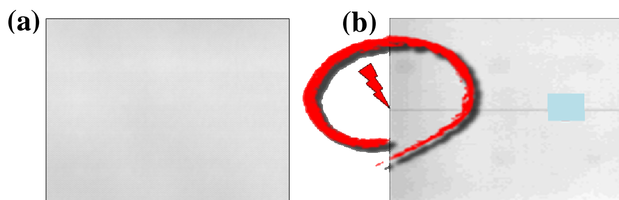

Fig. 3. The phenomenon of same panel during turned-on (a)normal image under normal driving and at R. T. (b)detected failure's image on ASG circuit which Burnt by Aging and HVS driving.

Fig. 4. shows the analytical result of failed TR that was detected as shorted common line and gate line. ASG circuits associated with horizontal black line were investigated in order to search failure points. Fig.4(a) shows microscope image of ASG circuit where a burnt TR is observed. If one of TRs is broken then the whole line including ASG circuit will be in failure. Fig. 4 (b) shows I-V characteristics of ASG output terminal. Damaged TR causes shorten ASG circuit, and abnormally huge leakage current flows at reverse bias region.

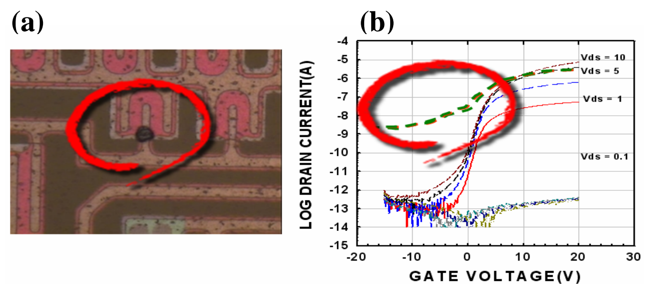

Fig.4. Analysis result (a) scope image of TR burnt (b) I-V Characteristic of failure's on ASG circuit

These results were obtained with DEMO version of cell aging tester in order to confirm the performance for aging condition. Immediately, we (have) designed the production equipment which could be acceptable for mass production.

Table 2. shows specifications of aging chamber. Temperature is controlled with (as) 0.1°C unit from room temperature to 65°C. It means that driving circuit including probe unit systems could guarantee the durability by 65°C. Also continuous operation time is guaranteed for 3,000 hours. Mini-heater with 1.5kw capacity attached to the side of the equipment. Capacity of temperature rising fan is 3.0m^2 per minute. It was automatically heated by using Temperature controller.

TABLE 2. Specification table of aging chamber

	Temp.	Operating time	FAN CAPA.	Heating Type
SPEC	60±5° C	3,000 hours (Max.)	3.0m^2 /min 106 CFM	Mini Heater (1.5 kw)

Fig. 5. shows the design for mass production which consists of aging chamber and test site. Fig. 5 (a) and (b) show top and side views of frame structure, where Fig. 5. (c) and (d) show side view of completed final

version with aging chamber docked. This equipment could perform eight panels or more at the same time. If someone needs more sites for aging test it is possible to insert more chambers and test sites.

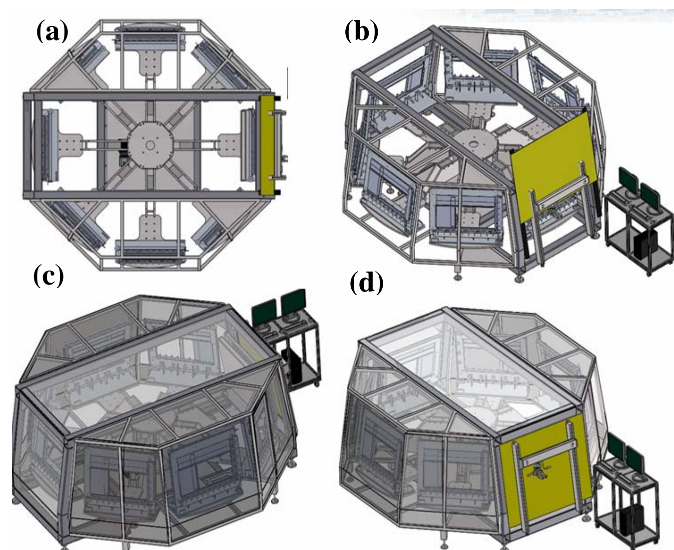

Fig. 5. Designs and lay-out of cell aging tester for mass production (a) top view (b) side view of frame structure(aging chamber-less), (c) and (d) side view of final version.

4. Summary

This study includes the development of a new apparatus and method of detecting for potential failures at the stage of LCD cell manufacturing. Demo version of cell aging tester revealed that the aging condition was appropriate for the detection of potential failure. The failure was attributed to the abnormal increase in leakage current of TR in an ASG circuit. Furthermore, it was applied for mass production by modifying the test equipment apparatus.

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