Advances in Zinc Oxide-Based Devices for Active Matrix Displays.

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Abstract

Metal oxides have been proposed as an alternative channel material to hydrogenated amorphous silicon in thin film transistors (TFTs) because their higher mobility and stability make them suitable for transistor active layers. Thin films of indium zinc oxide (IZO) were deposited using a High Target Utilization Sputtering (HiTUS) system on various dielectrics, some of which were also deposited with the HiTUS. Investigations into bottom-gated IZO TFTs have found mobilities of 8 cm²V ¹s⁻¹ and switching ratios of 10⁶. There is a variation in the threshold voltage dependent on both oxygen concentration, and dielectric choice. Silica, alumina and silicon nitride produced stable TFTs, whilst hafnia was found to break down as a result of the IZO.

1. Introduction

New large-area electronic technologies (such as active matrix addressed organic light emitting displays) require thin film transistors (TFTs) with greater stability and drive current at a lower processing temperature than hydrogenated amorphous silicon (a-Si:H) can currently provide.

One alternative is to use a metal oxide semiconductor as the transistor active layer. Metal oxides can be deposited by sputtering. However, in typical RF magnetron sputtering, it can be difficult to control the properties of the deposited material because the ion current and RF power are not independent of each other and because the deposited material is bombarded with ions. A recently developed sputtering method, the High Target Utilisation Sputtering (HiTUS) system prevents ion bombardment and separates the ion current and RF power by generating the plasma remotely. This has enabled fast

(>30 nm/min) deposition rates of metal oxide thin films in which the material properties can be precisely and reproducibly controlled. Consequently, the system can be used to fabricate all layers in a transparent TFT.

Indium Zinc Oxide (IZO) has been employed as the channel layer because of its particular advantages over a-Si:H. IZO has previously exhibited field effect mobilities in excess of 10 cm²V⁻¹s⁻¹, and order of magnitude greater than a-Si:H, and the inclusion of indium is thought to favour the deposition of a material with a disordered structure³. This suits large area applications because the lack of crystal grains results in uniformity of electronic behaviour across the substrate. Zinc oxide tends to form thin films with a polycrystalline structure which is thought to limit the device performance, with lower field effect mobilities (0.2 cm²V⁻¹s⁻¹) and lower on-off ratios (10⁴) determined by this method reported elsewhere⁴.

The choice of dielectric determines some of the properties of the device, particularly the threshold voltage and crucially, whether the device will work at all. This paper will outline typical IZO device characteristics and discuss the compatibility of IZO with four dielectrics: alumina, silica, hafnia and silicon nitride by examining their TFT characteristics.

2. Experimental details

Deposition of the layers was (with the exception of silicon nitride, deposited by plasma enhanced chemical vapor deposition (PECVD) and thermally grown silica) performed using the HiTUS system, a schematic diagram of which is shown in figure 1. The system generates an RF plasma remotely in the

sidearm, which is then confined and directed onto the target using electromagnets. Sputtering is achieved by separately applying a high dc voltage to the target, consequently decoupling the ion density (controlled by the RF power supply) and the ion energy (controlled by the target bias). Because of this independent control, the target-substrate separation can be increased, preventing ion bombardment of the substrate and deposited films.

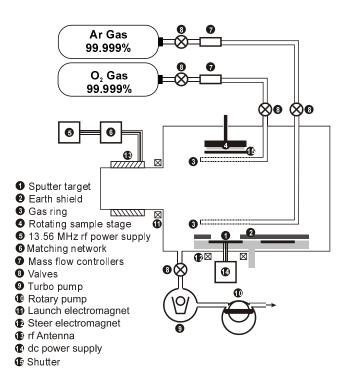


Fig. 1. A schematic diagram of the HiTUS sputtering system $^{\circ, \pm}$ ** $^{\circ, \pm}$

Oxide films were generated by reactive deposition, with oxygen injected into the chamber through a ring located around the substrate. Control over the partial pressures of oxygen and argon allows for control, in turn, over the properties of the deposited film. This enabled deposited alumina and hafnia to have resistivities of up 10^{16} and 10^{15} Ω cm respectively, with alumina exhibiting slightly better breakdown fields of 5 MV/cm. Depositions were typically carried out with target powers of ~1000 W and chamber pressures of 3-5×10⁻³ mBar. Both were deposited on Corning glass upon which 100 nm of indium tin oxide (ITO) had already been coated by standard rf magnetron sputtering to act as the gate. Meanwhile, 200 nm of silicon nitride (with a resistivity of 10^{13} Ω cm) was deposited onto highly n-doped silicon.

IZO channels of various dimensions were prepatterned by optical lithography, with lift-off defining the channels post-deposition. IZO was deposited from a bimetallic alloy target with an indium:zinc ratio of 10:90 at a lower target power of 500 W. This lower power was employed to ensure that the indium does not melt. The target gives IZO films in which the indium and zinc are in roughly equal amounts. This discrepancy is thought to be a result of the differing sputter thresholds for indium and zinc. ITO also formed the source and drain contacts and they were also defined by an optical lithography/lift-off process.

3. Results and Discussion

Figure 2a shows typical transfer characteristics of an IZO TFT with an alumina gate dielectric and a W/L of 100. The deposited TFT exhibits significant hysteresis and off-current with a low switching ratio of 10⁴. The field effect mobility was extracted to be 0.1 cm²V⁻¹s⁻¹. Figure 2b shows the same device after annealing at 200 °C for one hour.

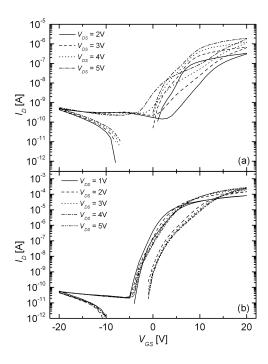


Fig. 2. Gate transfer characteristics for (a) preannealed and (b) post-annealed IZO TFTs with an alumina dielectric.

Annealed devices experienced a decrease in the hysteresis, an increase in the on-current, an increase in the switching ratio to 10⁶ and a decrease in the off-

current. The field-effect mobility was extracted to be 2.2 cm²V⁻¹s⁻¹, a little less than the maximum achieved, which can be attributed to the particularly high oxygen content in the IZO semiconductor used for this particular device. Indeed, an increase in the threshold voltage and a decrease in mobility with increasing oxygen content in the IZO film was observed throughout. When the IZO semiconductor was deposited using a lower oxygen content, the resulting TFT showed a much improved mobility of 8 cm²V⁻¹s⁻¹.

TABLE 1. Threshold voltages before and after annealing for different dielectrics for similar IZO channels.

Threshold voltage / V	SiO_2	AlO_x
Before annealing	31	5
After annealing	3	11

Annealing is thought to remove water added to the films during lithographical steps. This is thought to be independent of gate dielectric choice, since all functioning dielectrics exhibited hysteresis and threshold voltage shifts after annealing. What did vary between dielectrics was the threshold voltage. Before annealing, TFTs with silica dielectrics had threshold voltages of around 30 V, whilst TFTs with alumina dielectrics exhibited threshold voltages around zero (though both showed large hysteresis). After annealing, TFTs with silica dielectrics were found to be close to zero, whilst the alumina increased to 10 V. Table 1 details typical threshold voltages before and after annealing for TFTs with similar IZO channels but with different gate dielectrics.

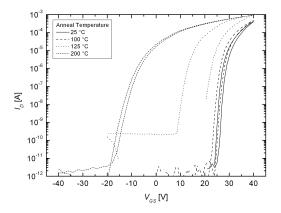


Fig. 3. Gate transfer characteristics as a function of annealing temperature for IZO TFTs with a silica dielectric.

The fact that the direction of threshold voltage change before and after annealing varies between dielectrics indicates that the IZO-dielectric interface plays a key role in device characteristics. Interestingly, after leaving the devices for a number of weeks in air, the devices began to return to their previous state. This again strongly points to water adsorption/absorption rather than structural changes. Conversely, modest heating reveals transition states in the gate transfer characteristics. Figure 3 shows an IZO device with a SiO₂ dielectric and the variation of the gate transfer with annealing temperature. This process is reversible. More importantly, a straightforward passivation layer should remove this effect.

Leakage current was found to be small for both alumina and silica, with most devices exhibiting leakage in the 10s of pA range.

TFTs with a hafnia dielectric had very low breakdown voltages (<3 V). It is postulated that this is because of a reaction (or diffusion) of the indium with the hafnia producing conduction pathways and/or a small band offset between the IZO and the hafnia. This has been estimated from an extensive survey of literature, and was extended to cover all the dielectrics covered in this paper. Assuming a 50% contribution of indium oxide^{5,6} and zinc oxide⁷, the band offsets were calculated using literature values for dielectrics⁸ and are detailed in Table 2.

TABLE 2. Band offset calculations for IZO and various gate dielectrics.

Offsets / eV	SiO_2	AlO_x	HfO_x	SiN_x
Conduction Band	2.61	2.51	1.01	1.41
Valence Band	2.97	2.87	1.57	0.47

Whilst it is accepted that the values in Table 2 are only estimates, clearly silica and alumina offer the best choice of dielectric with IZO as has already been clearly demonstrated. To make hafnia work more effectively, perhaps a thin passivation layer may be required between the hafnia and the IZO for the benefits of hafnia to be realized.

 $\mathrm{SiN_x}$ dielectrics produced stable current-voltage characteristics, but exhibited a higher gate leakage than alumina and silica because of its lower resistivity. Whilst the two are compatible, it is more convenient to deposit two layers with one process.

4. Summary

Metal oxides deposited by the HiTUS method have produced high-mobility transparent TFTs. IZO has been found to be compatible with a variety of dielectrics, although the dielectrics which gave the best performance were alumina and silica. Both exhibited leakage currents of the order of 10s of pA. Hafnia, whilst previously shown to be compatible with ZnO, was not found to be compatible with IZO and, following band off-set calculations, 1 eV may be too small a barrier to suppress gate leakage currents and to prevent dielectric breakdown. SiN_x deposited PECVD also produced reasonable characteristics, but it may be more economical to deposit all layers by the same method for future applications. Regarding future applications, metal oxide TFTs are promising candidates to drive active matrix displays.

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