Novel Direct Duty-Ratio Modulation Method for Matrix Converter

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Abstract

A novel general direct duty ratio pulse width modulation strategy is proposed to modulate matrix converters. By using average concept over one switching period, the modulation algorithm and the required equations are derived to synthesize the desired output voltage and to achieve the controlled input power factor. The proposed method use continuous carrier and the predetermined duty ratio signal for directly generating gating signals an thus is named "direct duty ratio PWM(DDPWM)".The feasibility and validity of the proposed strategy are verified by experimental results.

1. Introduction

Direct AC-AC converters based on matrix converter topology have been the researching interesting in recent years. Matrix converter contains an array of controlled semiconductor switches. These switches are forced on or off to generate desired output voltages with controllable input power factor [1]. Three major modulation techniques are developed to control the three-phase to three-phase matrix converters; Alesina–Venturini method [2], space vector pulse width modulation(PWM) [3] and carrier based PWM [4]. However, Alesina–Venturini method and space vector PWM are not easy to implement because of requirement of complex calculation or lookup table initialization. The carrier based PWM in [4] implies relatively indirect understanding of matrix converter modulation because it involves discontinuous carrier waveform.

This paper presents a direct duty ratio PWM method for matrix converters, which is a carrier based PWM with continuous triangular carrier waveform [5]. The proposed method generates proper duty-ratios to directly control a three-phase matrix converter. It can be easily implemented without complex calculation and lookup table. The proposed method also has good feasibility and can be applied to effectively control the two-phase and three-phase four-leg matrix converters. It offers a simple and direct way to understand the modulation process of matrix converters.

2. Proposed DDPWM Method

2.1 Proposed DDPWM controller

Fig. 1 shows the circuit configuration including the three-phase input voltages, input filter, three-phase to three-phase matrix converter and resister-inductor(R-L) load.

If the only maximum one of the three line-to-line voltages is used as the input voltage to synthesize the output voltages during each switching period, then two of the three input phase voltages will be used. Consequently, one of the input phases does not conduct any current during the switching period, so that the input current will be distorted. The DDPWM uses two out of three of the line-to-line input voltages to synthesize the output voltages. Hence, all three input phases are utilized to conduct current during each switching period and, consequently, the input currents will not be distorted.

A switching period T_s can be divided into two sub-intervals, T_1 and T_2. Also, the maximum, medium and minimum input voltage values are designated as *MX*, *MD* and *MN* respectively.

During T_1, the line-to-line voltage between *MX* and *MN*, which is the maximum line-to-line voltage among the three line-to-line input voltages at the sampling instant, is used. During T_2, the second maximum line-to-line voltage, which is the larger one in *MX* to *MD* and *MD* to *MN*, is used. If *MX-MD*>*MD-MN*, *MX* to *MD* is used in T_2 and the switching pattern is named as switching pattern-I. Otherwise, if *MD* to *MN* is used in T_2, it is named as switching pattern-II.

Switching pattern-I: Fig. 2 shows the case of switching pattern-I for generating the *A*-phase output voltage, where the triangular carrier is compared with the duty ratio value, d_{A1}, resulting in the change of the output phase voltage such that *MN*→*MX*→*MD*. Fig. 2 shows the actual *A*-phase output voltage synthesis when applying switching pattern-I. As seen in Fig. 2, *MN*, *MX*, *MX* and *MD* appear at the *A*-phase output terminal during T_{A1}, T_{A2}, T_{A3} and T_{A4} respectively. These four sub-intervals can be expressed as

$$\begin{aligned} T_{A1} &= d_{A1} n T_s \\ T_{A2} &= (1-d_{A1}) n T_s \\ T_{A3} &= (1-d_{A1})(1-n) T_s \\ T_{A4} &= d_{A1}(1-n) T_s \end{aligned} \tag{1}$$

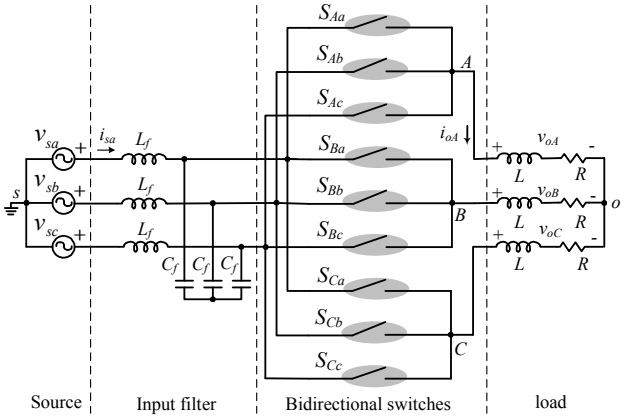

Fig. 1 Three-phase to three-phase matrix converter circuit.

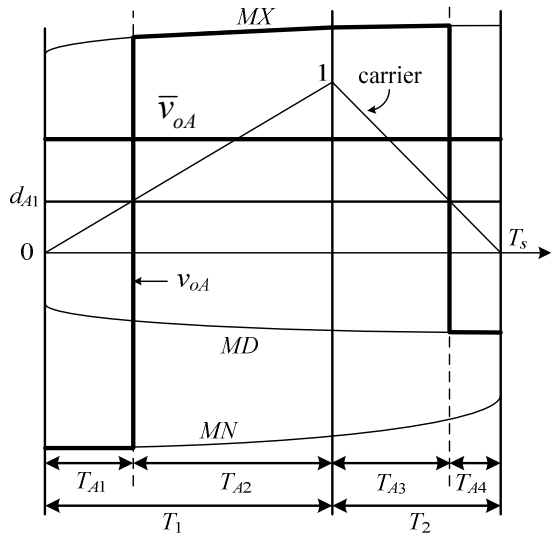

Fig. 2 Output *A*-phase voltage synthesis in switching pattern-I.

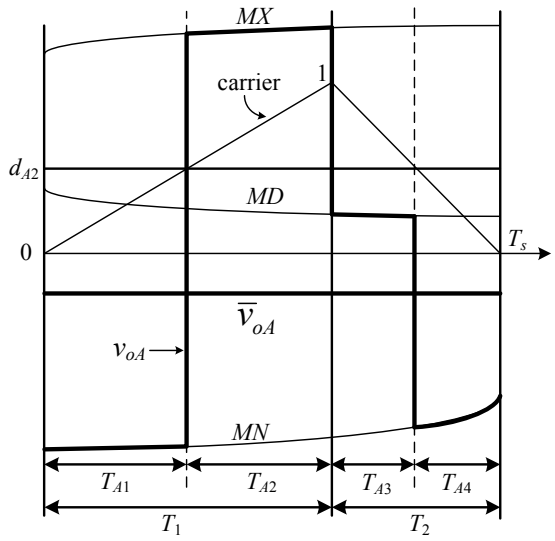

Fig. 3 Output *A*-phase voltage synthesis in switching pattern-II.

where d_{A1} is the *A*-phase duty ratio value when switching pattern-I is applied and n is defined as $n = T_1/T_s$ which involves the slope of the carrier.

Supposing that the input voltages are almost constant during the switching cycles, the integration of the output voltage v_{oA} over T_s can be written as

$$\int_0^{T_s} v_{oA}\, dt \;\cong\; T_{A1}\cdot MN + \left(T_{A2}+T_{A3}\right)\cdot MX + T_{A4}\cdot MD \tag{2}$$

Then, it is found from (1) and (2) that the averaged value of v_{oA}, $\overline{v}_{oA}$, can be approximated by

$$\begin{aligned}\overline{v}_{oA} &= \frac{1}{T_s}\int_0^{T_s} v_{oA}\,dt \\ &\cong\; d_{A1}\left(n\cdot MN - n\cdot MD + MD - MX\right) + MX\end{aligned} \tag{3}$$

By letting $\overline{v}_{oA}$ be equal to the *A*-phase output voltage command, v_{oA}^*, that is $\overline{v}_{oA} = v_{oA}^*$, then the duty ratio value, d_{A1}, for the present switching period can be calculated as

$$d_{A1} = \frac{1}{n\cdot MN - n\cdot MD + MD - MX}\left(v_{oA}^* - MX\right) \tag{4}$$

Switching pattern-II: In the same way, switching pattern-II can be analyzed. Fig. 3 shows the case of switching pattern-II for generating the *A*-phase output voltage where the triangular carrier is compared with the duty ratio value, d_{A2}, so that the time intervals, viz. T_{A1}, T_{A2}, T_{A3} and T_{A4}, are predetermined as given in equation (1) and the output phase voltage is changed with the sequence of *MN*→*MX*→*MD*→*MN*. When applying switching pattern-II, the *A*-phase output voltage is actually synthesized as shown in Fig. 3. As seen in Fig. 3, *MN*, *MX*, *MD* and *MN* appear sequentially at the *A*-phase output terminal. In this case, the integration of the output voltage v_{oA} over T_s is expressed by

$$\int_0^{T_s} v_{oA}dt \;\cong\; T_{A1}\cdot MN + T_{A2}\cdot MX + T_{A3}\cdot MD + T_{A4}\cdot MN \tag{5}$$

Similarly, it can be found from (1) and (5) that the averaged value of v_{oA}, $\overline{v}_{oA}$, can be approximated by

$$\begin{aligned}\overline{v}_{oA} &= \frac{1}{T_s}\int_0^{T_s} v_{oA}\,dt \\ &\cong\; d_{A2}\cdot\left(MN - n\cdot MX - MD + n\cdot MD\right) \\ &\quad + n\cdot MX - n\cdot MD + MD\end{aligned} \tag{6}$$

Again, by letting $\overline{v}_{oA}$ be equal to the *A*-phase output voltage command, v_{oA}^*, the duty ratio value, d_{A2}, can be obtained as follows

$$d_{A2} = \frac{v_{oA}^* - \left(n\cdot MX - n\cdot MD + MD\right)}{MN - n\cdot MX - MD + n\cdot MD} \tag{7}$$

In summary, the duty ratio value d_A for *A*-phase at each switching cycle is determined by

$$d_A = \begin{cases} \dfrac{v_{oA}^* - MX}{n\cdot MN - n\cdot MD + MD - MX} & \text{for Pattern-I} \\[2ex] \dfrac{v_{oA}^* - \left(n\cdot MX - n\cdot MD + MD\right)}{MN - n\cdot MX - MD + n\cdot MD} & \text{for Pattern-II} \end{cases} \tag{8}$$

The duty ratio control law of the *A*-phase output is defined by (8). The other two output phases can be treated in the same manner. It should be noticed that the three output phase voltages can be separately controlled to follow their own references. This fact implies that the DDPWM controller can be implemented with a modular structure for each phase.

2.2 Input current synthesis

In the global duty ratio laws in (8), there is another degree of freedom, that is n. n can be properly adjusted to synthesize the sinusoidal input current, while maintaining T_s at a constant value. Since n is already considered in the derivation of (8), the output voltage synthesis will not be disturbed by changing the value of n. Under the condition of unit power factor, it can be found that n is determined by

$$n = \begin{cases} -MN/MX & \text{pattern-I} \\ -MX/MN & \text{pattern-II} \end{cases} \tag{9}$$

2.3 Analysis of available voltage conversion range

In the DDPWM, the controller properly organizes the three input phase voltages so as to generate the desired output voltages directly. The maximum of output voltages should be smaller than the minimum of input voltages. Hence, the conversion ratio q may be limited to 0.5 at specific range. In order to expand q to 0.866, the DDPWM utilize the output voltage references including third harmonics terms as given in [2].

The three output phase voltage commands can be given as

$$v_{oA}^{*} = V_o \sin(\omega_o t) - \frac{\sqrt{6}}{12} V_{s-\mathrm{RMS}} \sin(6\pi f_i t) + \frac{1}{6} V_o \sin(6\pi f_o t)$$

$$v_{oB}^{*} = V_o \sin\left(\omega_o t - \frac{2\pi}{3}\right) - \frac{\sqrt{6}}{12} V_{s-\mathrm{RMS}} \sin(6\pi f_i t) + \frac{1}{6} V_o \sin(6\pi f_o t)$$

$$v_{oC}^{*} = V_o \sin\left(\omega_o t + \frac{2\pi}{3}\right) - \frac{\sqrt{6}}{12} V_{s-\mathrm{RMS}} \sin(6\pi f_i t) + \frac{1}{6} V_o \sin(6\pi f_o t) \quad (32)$$

where v_{oB}^{*} and v_{oC}^{*} are the output *B*-phase and *C*-phase command respectively. V_o is the output voltage magnitude, $V_{s\text{-RMS}}$ the input line-to-line RMS voltage, ω_o output angular frequency, f_i input frequency and f_o output frequency.

3. Experiment

To verify the feasibility of the proposed DDPWM methods, an experimental setup was built and the DDPWM controller was implemented by using TMS320VC33 DSP from Texas Instruments and Altera CPLD of EP1K100QC208-1. The experimental conditions are given in Table 1. The experimental configuration is shown in Fig. 4. As seen in Fig. 4, two out of three input line-to-line voltages v_{sab} and v_{sbc} are sensed in order to calculate three input phase voltages v_{sa}, v_{sb} and v_{sc}. Sampled values of v_{sa}, v_{sb} and v_{sc} are then used to needed calculation. Input phase locked loop (PLL) is also incorporated into DSP to obtain input voltage angle α_i and to determine the proper switching pattern. Three input phase currents i_{sa}, i_{sb}, i_{sc} are sensed only for protection purpose. Three output phase currents i_{oA}, i_{oB} and i_{oC} are sensed for both control and protection purpose.

The steady state experimental waveforms are shown in Fig. 5, when q=0.866 and f_o=30Hz. Fig. 5 contains the steady state experimental waveforms of the output line-to-line voltage v_{oAB}, output current i_{oA}, input voltage v_{sa} and input current i_{sa}. In Fig. 5,

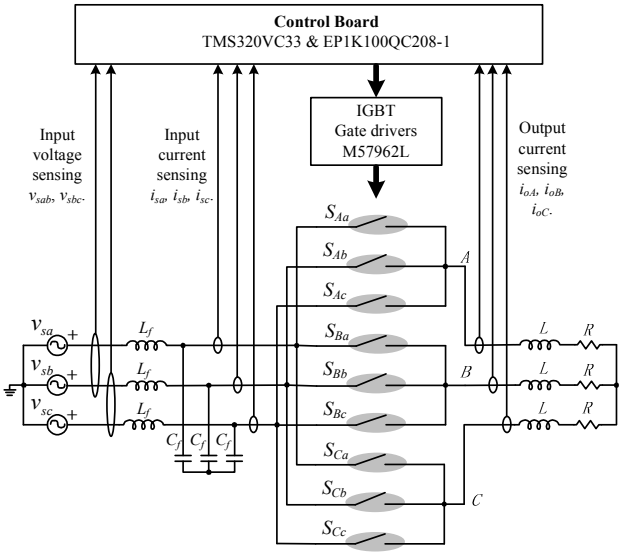

Fig. 4 Configuration of experimental setup

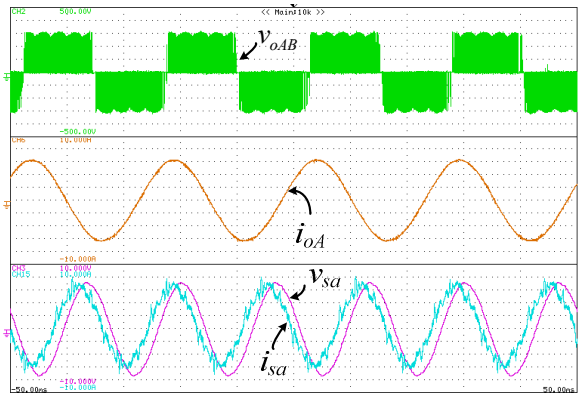

Fig. 5 Experimental waveforms: steady state operation
v_{oAB} (100V/div, 10ms/div),i_{oA}(2A/div, 10ms/div)
v_{sa}(50V/div, 10ms/div),i_{sa}(2A/div, 10ms/div)

Table 1 Experimental parameters

Rated Input voltage $V_{s\text{-RMS}}$	220V
Input filter L_f, C_f	100μH, 60μF
R-L load	20Ω-50mH
Input frequency f_i	60Hz
Switching frequency f_s	5kHz

i_{sa} shows a small phase difference with the leading power factor, because of the input filter. It can be confirmed that the proposed DDPWM method is able to effectively synthesize both the output voltage and input current while achieving unity input power factor.

4. Conclusions

This paper presents a novel DDPWM based on the use of a continuous carrier to modulate matrix converters. The experimental results show that both the output voltages and input currents can be effectively modulated. It can be concluded that the proposed method offers a very simple and effective way to modulate matrix converters.

Acknowledgment

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Reference

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