Novel two phase interleaved LLC series resonant converter using a phase of the resonant capacitor

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***Abstract*— LLC series resonant converter has many unique characteristics and improvement over PWM topologies. However, many output capacitors should be needed in parallel to satisfy an output voltage ripple and a rated ripple current of the capacitors. This paper is deal with a novel two phase interleaved LLC resonant converter using a phase of the resonant capacitor. The proposed converter can satisfy output voltage ripple and a rated ripple current of capacitors with few output capacitors, relatively. The operation and features is considered in detail and a prototype with a 12V-100A output is investigated.**

***Index Terms*— LLC series resonant converter, Phase of the resonant capacitor, Interleaving operation**

1. INTRODUCTION

Due to high power density requirement, high frequency DC/DC power converters are employed increasingly in many applications. People pay more attention to the LLC series resonant converter (LLC-SRC), owning to its many unique characteristics and improvements over previous PWM converters. For example, it has simple structure and could achieve primary MOSFETs' zero voltage switching (ZVS) and the secondary rectifiers' zero current switching (ZCS) from no load to full load [1]. However, many output capacitors in the conventional LLC-SRC should be needed in parallel to satisfy an output voltage ripple and a rated ripple current of capacitors because the secondary current is discontinuous and the peak current value is large. In addition, this problem is very serious in high current output applications. Although a high frequency operation can be a solution for reducing the output capacitance, many capacitors in parallel are still needed to satisfy a rated ripple current of the output capacitor.

An interleaved operation can be the solution for this drawback but the complex controller is needed to obtain the interleaving operation in the prior approach [2]. In this paper, a new interleaved LLC-SRC is proposed without the complicated controller. It is suitable for the low-voltage and high-current application, which is using the synchronous switch to reduce the Schottky diode's conduction loss. The interleaved operation in the proposed converter can be easily obtained without the complex controller because it simply uses a phase of the resonant capacitor. Furthermore, the output capacitor and the conduction loss can be reduced by the interleaved operation. As a result, the proposed converter can achieve the high efficiency, the high power density and the low cost. The method of using a phase of the resonant capacitor can be extended to make multi-phase interleaved LLC-SRC.

2. THE PROPOSED CONVERTER

Fig. 1 shows the circuit diagram and key waveforms of the proposed two phase interleaved LLC-SRC. The proposed converter is composed of two half-bridge LLC-SRCs, which one is master converter and the other is slave converter. The gate signals of the MOSFET in the master converter are made by the conventional controller to regulate the output power and the gate signals of the slave converter are made by a phase of resonant capacitor, C_{r1}, voltage in the master converter as shown in Fig. 1 (a). Since the phase between the resonant inductor current and the resonant capacitor voltage has 90 degree difference, the interleaving operation in the master and the slave converters can be easily obtained by detection of the phase of the resonant capacitor voltage, v_{Cr1}. The operational principle of the proposed circuit can be explained as follows. The operation of the proposed circuit can be divided to eight modes. Since M1~M4 and M5~M8 are symmetric, the operation from M1 to M4 will be explained. It is assumed that the components in the master and slave converter are ideally same.

Mode 1(t_0~ t_1): *S*witches, M_1 and M_2', have been turned on and the energy is transferred from input to output by the master and slave converter. The inductor currents can be expressed as follows

$$i_{Lr1}(t) = I_{Lr1}(t_0)\cos\frac{1}{\sqrt{L_{r1}C_{r1}}}(t-t_0) + \left(V_{in}/2 - V_{Cr1}(t_0)\right)\Big/\sqrt{\frac{L_{r1}}{C_{r1}}}\sin\frac{1}{\sqrt{L_{r1}C_{r1}}}(t-t_0) \tag{1}$$

$$i_{Lr2}(t) = I_{Lr2}(t_0)\cos\frac{1}{\sqrt{L_{r2}C_{r2}}}(t-t_0) - \left(V_{in}/2 - V_{Cr2}(t_4)\right)\Big/\sqrt{\frac{L_{r2}}{C_{r2}}}\sin\frac{1}{\sqrt{L_{r2}C_{r2}}}(t-t_0) \tag{2}$$

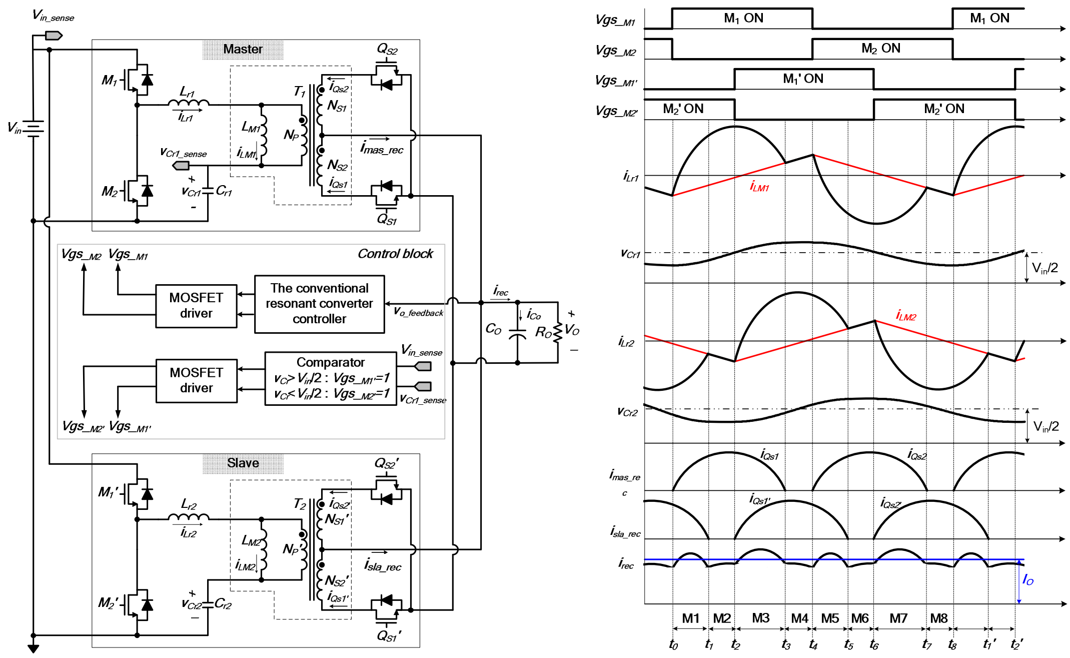
where $I_{Lr1}(t_0) = I_{Lr2}(t_0) = I_{Lm,peak}$.

Mode 2(t_1~ t_2): The master converter only transfers the energy to the output because the resonance between L_{r2} and C_{r2} has been completed in the slave converter. The primary currents can be obtained as follows.

$$i_{Lr1}(t) = I_{Lr1}(t_0)\cos\frac{1}{\sqrt{L_{r1}C_{r1}}}(t-t_0) + \left(V_{in}/2 - V_{Cr1}(t_0)\right)\Big/\sqrt{\frac{L_{r1}}{C_{r1}}}\sin\frac{1}{\sqrt{L_{r1}C_{r1}}}(t-t_0) \tag{3}$$

$$i_{Lr2}(t) = I_{Lr2}(t_1)\cos\frac{1}{\sqrt{(L_{r2}+L_{m2})C_{r2}}}(t-t_1) - V_{Cr2}(t_1)\Big/\sqrt{\frac{(L_{r2}+L_{m2})}{C_{r2}}}\sin\frac{1}{\sqrt{(L_{r2}+L_{m2})C_{r2}}}(t-t_1) \tag{4}$$

Mode 3(t_2~ t_3): When the v_{Cr1} is over $V_{in}/2$ in the master converter,



(a) (b)

Fig. 1. Proposed two phase interleaved LLC-SRC

(a) Circuit diagram (b) Key waveforms

the M1′ switch is turned on and the output is also made by slave converter with the master converter.

$$i_{Lr1}(t)=I_{Lr1}(t_0)\cos\frac{1}{\sqrt{L_{r1}C_{r1}}}(t-t_0)+\left(V_{in}/2-V_{Cr1}(t_0)\right)\Big/\sqrt{\frac{L_{r1}}{C_{r1}}}\sin\frac{1}{\sqrt{L_{r1}C_{r1}}}(t-t_0) \quad (5)$$

$$i_{Lr2}(t)=I_{Lr2}(t_2)\cos\frac{1}{\sqrt{L_{r2}C_{r2}}}(t-t_2)+\left(V_{in}/2-V_{Cr2}(t_2)\right)\Big/\sqrt{\frac{L_{r2}}{C_{r2}}}\sin\frac{1}{\sqrt{L_{r2}C_{r2}}}(t-t_2) \quad (6)$$

Mode 4(t_3~ t_4): Since the resonance between L_{r1} and C_{r1} is finished in the master circuit, the slave converter only transfers the energy to the output.

$$i_{Lr1}(t)=I_{Lr1}(t_3)\cos\frac{1}{\sqrt{(L_{r1}+L_{m1})C_{r1}}}(t-t_3)+\left(V_{in}-V_{Cr1}(t_0)\right)\Big/\sqrt{\frac{(L_{r1}+L_{m1})}{C_{r1}}}\sin\frac{1}{\sqrt{(L_{r1}+L_{m1})C_{r1}}}(t-t_3) \quad (7)$$

$$i_{Lr2}(t)=I_{Lr2}(t_2)\cos\frac{1}{\sqrt{L_{r2}C_{r2}}}(t-t_2)+\left(V_{in}/2-V_{Cr2}(t_2)\right)\Big/\sqrt{\frac{L_{r2}}{C_{r2}}}\sin\frac{1}{\sqrt{L_{r2}C_{r2}}}(t-t_2) \quad (8)$$

The primary switches in the slave converter are easily driven by comparison between the input and the resonant capacitor voltages in the master converter. Furthermore, different from the conventional LLC-SRC, the current, i_{rec}, is continuous in the proposed converter as shown in Fig. 1. It results in the reduction of output voltage ripple and a root mean square (RMS) value of the output capacitor's ripple current. The peak value of the rectified current and the RMS values of the output capacitor's ripple currents of the conventional full-bridge LLC-SRC and the proposed converter can be obtained during a half of the switching period as follows

$$I_{Conventional\_rec\_pk}\cong\frac{T_S}{T_r}\frac{\pi}{2}I_o \quad (9)$$

$$I_{Conventional\_Co\_RMS}\cong I_o\sqrt{\left(\frac{\pi^2}{8}\frac{T_S}{T_r}-1\right)} \quad (10)$$

$$I_{Proposed\_rec\_pk}\cong\frac{T_S}{T_r}\frac{\pi}{4}\sqrt{2}I_o \quad (11)$$

$$I_{Proposed\_Co\_RMS}\cong I_o\sqrt{\left(\frac{\pi^2}{16}\frac{T_S}{T_r}\left(1+\frac{2}{\pi}\right)+\frac{T_r}{T_S}-2\right)} \quad (12)$$

where T_s is the switching period, T_r is the resonant period and ω_r is $2\pi/T_r$.

By (9)-(12), the peak value of the rectified current and the RMS value of the output capacitor's ripple current can be obtained according to the output current as shown in Fig.2. Fig. 2 illustrates that the proposed circuit has the greatly reduced peak value of the rectified current and the RMS value of the output capacitor current. Since the RMS value of the output capacitor ripple current will not be decreased with the high frequency operation, the many electrolytic capacitors are parallel needed to satisfying the rated ripple current of the output capacitor in the conventional LLC-SRC. However, since the rectified current of the proposed circuit is continuous, the peak value of the rectified current, the ripple current and the RMS value of the output capacitor are small, respectively. Thus, the proposed circuit can have fewer output capacitors and the smaller conduction losses in the transformer and the synchronous MOSFET. Therefore, the proposed circuit can obtain the high power density, high efficiency and the low cost.

3. Experimental Results

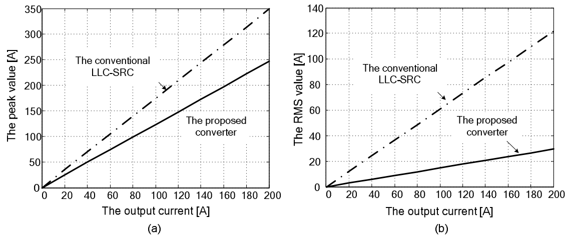


Fig. 2 Comparison in the prior and the proposed circuit
(a) The peak value of the rectified current
(b) The RMS value of the output capacitor ripple current

TABLE I
SPECIFIC COMPONENTS OF A PROTOTYPE

Parameters	Symbol	Value/Part
Input voltage	V_{in}	410V
Output voltage	V_O	12V
Max. power rating	P_{max}	1200W
Turn ratio	N_p:N_{s1}:N_{s2}	16:1:1
Resonant inductor	L_r,$L_{r'}$	25uH
Magnetizing inductance	L_m, $L_{m'}$	1mH
Resonant capacitor	C_r, $C_{r'}$	63nF/600V
Output capacitance	C_o	330uF/(16V, 6.1Arms)(4EA)
Primary switches	$M_{1,2,1',2'}$	SPP20N60C3
Synchronous rectifier	$Q_{s1,s2,s1',s2'}$	IRF2804(2EA)
Synchronous rectifier driver		IR21167
Resonant mode controller		MC33067

A prototype of a 12V, 1.2kW converter with 410V input has been built for the application of the distributed power system of the server computer. The components are shown in table 1. The primary switches in the master converter are driven by the controller, which is used to regulate the output power and those in the slave converter are simply driven by comparison between the input voltage and the resonant capacitor voltage of the master converter. Fig. 3 shows the resonant inductor currents in the master and slave converter with the load variation. It is noted that the phase difference between the master's inductor current and the slave's one is about 90 degree and the input power is well divided to make the output power in the master and salve converts. Fig.4 shows the ripple output voltage capacitors in the 100A load. The peak to peak value of that is about 40mV with the four output capacitors due to the interleaving operation. Also, since the RMS value of the output capacitor current is small, the 4 capacitors is only needed to satify the rated ripple current of the electrolytic capacitor while the conventional LLC needed about the 12 capacitors. Fig 5 shows the efficiency of the proposed circuit according to the load variation. From the light load to the full load, the proposed converter has high efficiency over 90%. Using the phase of the resonant capacitor, the interleaved operation can be easily obtained without the compltcated controller. Due to this concept, the proposed LLC-SRC can have fewer output capacitors, higher efficiency and higher power density.

4. CONCLUSION

The proposed converter has the interleaved operation using a phase of the resonant capacitor and there is no complex controller. It also significantly reduces the RMS value of the output capacitor's current and the peak current value in the secondary side. This results in reducing the number of the output capacitors. Moreover, the method of using a phase of the resonant capacitor voltage can be extended to make multi-phase interleaved LLC-SRC. Therefore, it is suitable for a low voltage and a high current application such as server and telecommunication equipment that require high efficiency, high power density and low cost.

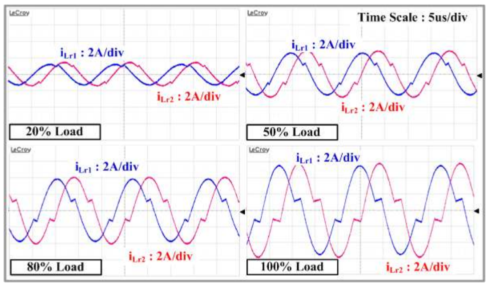


Fig. 3 The resonant inductor current with the load variation

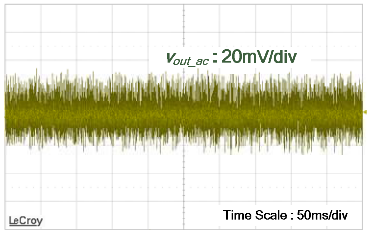


Fig. 4 The waveform of the ripple output voltage

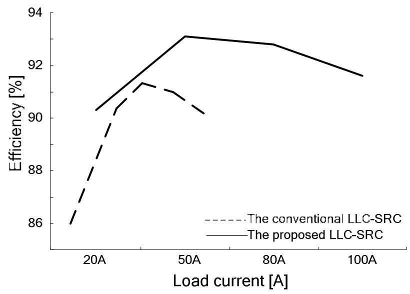


Fig. 5 Efficiency with load variation

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