Zero-Voltage Switching Dual Inductor-fed DC-DC Converter Integrated with Parallel Boost Converter

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Abstract

Novel zero-voltage switching(ZVS) dual inductor-fed DC-DC converter integrating a conventional dual inductor-fed boost converter(DIFBC) and a parallel bidirectional boost converter has been proposed. Most of current-fed type boost topologies including dual inductor schemes have crucial defects such as a high voltage spike on the main switch when it comes to turning off, an unattainable soft start-up due to the limited range of duty ratio, above 50%, and considerable switching losses due to the hard switching. By adding two auxiliary switches and an output capacitor on the conventional DIFBC, the proposed circuit can solve mentioned problems and improve the efficiency with simple methods. The operational principle and theoretical analysis of the proposed converter have been included. Experimental results based on a 42V input, 400V/1A output and 50kHz prototype are shown to verify the proposed scheme.

1. Introduction

With the demand for high step-up, high efficiency, and high power density in the DC/DC converter for the front-end stage of the battery, uninterrupted power supply, and fuel cell power system, current-fed topologies employing boost inductors at the primary side are widely used.

Among various current-fed type PWM DC/DC converters, the dual inductor-fed boost converter(DIFBC) is widely researched and used in medium-to-high power step-up applications because of its higher voltage gain than other current-fed step-up converters due to the voltage doubling effect. However, most of current-fed type boost topologies including dual-inductor schemes have crucial drawbacks.

At first, when a switch is turned off, high voltage oscillation between drain and source is produced due to the resonance between a transformer's leakage inductance and a switch's output capacitance. To protect switches from high voltage spikes, additional clamping circuits resulting extra losses such as a RCD snubber are required to absorb this surge energy as shown in Fig.1(a).

At second, the absence of boost inductors' current paths when two switches are turned off simultaneously causes in-rush current to start the converter. A soft start-up without severe in-rush current can be achieved by magnetically coupling the boost inductors toward the load as shown in Fig.1(a).

Modified DIFBC I is one of the reasonable approaches to solve mentioned problems as well as keeping advantages such as higher voltage gain than push-pull and full-bridge's. But additional clamping circuits and auxiliary coupling windings result in a complicated and bulky system.

To solve all these drawbacks and complexities, modified DIFBC II as shown in Fig. 1(b) has been proposed.[1] Due to the connected parallel boost diodes(D5, D6), the modified DIFBC II can solve the above mentioned problems alternatively and enhance the total efficiency. However, the modified DIFBC I and II cannot achieve ZVS, which causes switching losses. Thus, a novel ZVS DIFBC is proposed as shown in Fig. 2.

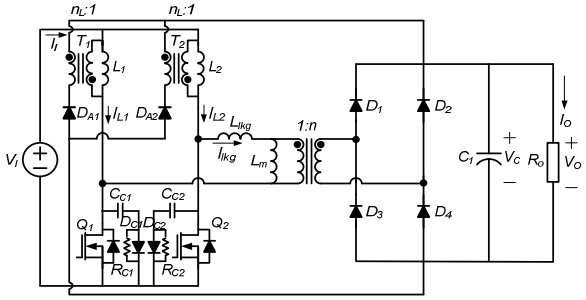


Fig. 1(a) Modified DIFBC I.

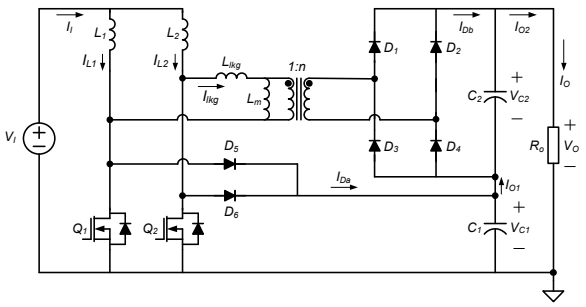


Fig. 1(b) Modified DIFBC II.

2. The Proposed Converter

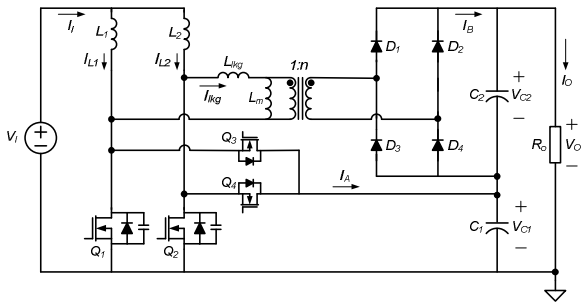


Fig. 2 The proposed converter.

The proposed circuit has the series-connected output configuration. Thus, average currents into each output capacitors are the same at the steady state.

$$I_O =< I_A >=< I_B > \quad (1)$$

$$V_O = V_{C1} + V_{C2} \quad (2)$$

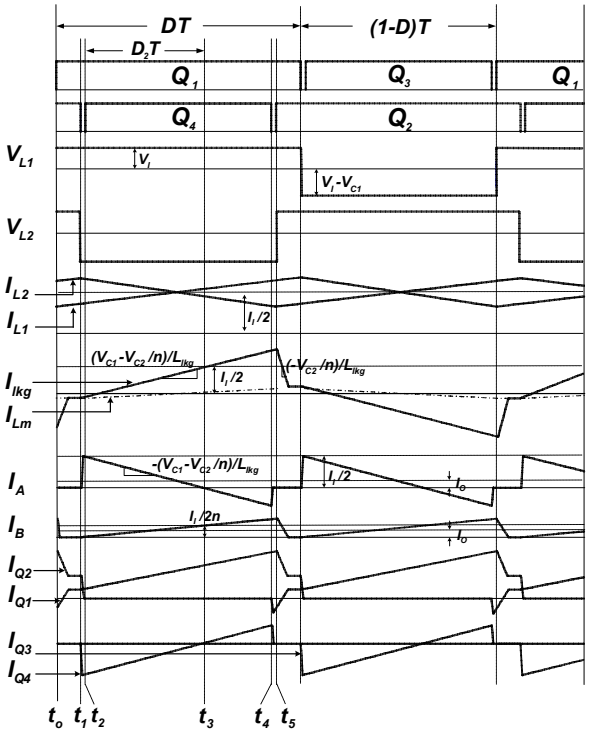
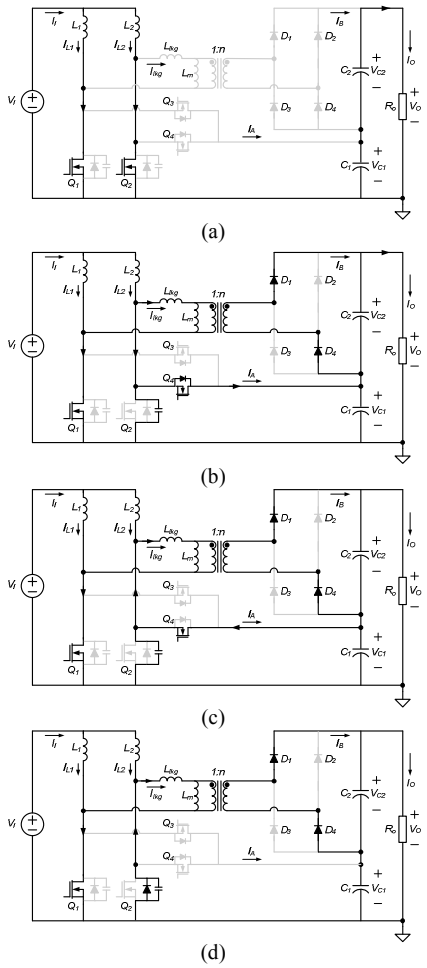


Fig. 3 Key waveforms of the proposed converter.



(a) Mode 1 (b) Mode 2 and 3 (c) Mode 4 (d) Mode 5

Fig. 4 Operational modes in a half duty cycle.

Equation (1) implies that divided average currents into two powering paths at the primary side can be determined by the ratio of n to 1.

2.1 Operational Principle

Mode 1(t_0~t_1): After Q_1 is turned on under ZVS conditions at t_0 while Q_2 has been turned on, Mode 1 begins. I_{L1} and I_{L2} are increased with linearly positive slope as shown in Fig. 3 for boosting operation, which stores the energy. Since there is no powering path, C_1 and C_2 discharge simultaneously.

Mode 2(t_1~t_2): After Q_2 is turned off at t_1, Mode 2 begins. I_{L2} charges C_1 and C_2 through two powering paths, I_{lkg} and I_A, simultaneously.

Since anti-parallel body diode of Q_4 is conducted right after turning Q_2 off, turn-off voltage across Q_2 is limited to V_{C1}. Thus additional dissipative clamping circuits are not required. A connected parallel boost converter plays a role of powering to the load as well as clamping turn-off switch's voltage in this mode. It also decreases turn-on switch's current stress by reducing current oscillations and allows lower voltage and current ratings' power MOSFETs having smaller drain-source resistance (R_{dsON}). Eventually it contributes to enhance the total efficiency with lessening switches' conduction loss.

Mode 3(t_2~t_3): Q_4 is turned on under ZVS conditions at t_2 while the anti-parallel body diode of Q_4 has been conducted. Due to the leakage inductance of the transformer, I_{lkg} increases and I_A decreases linearly with a slope of $\pm(V_{C1}-V_{C2}/n)/L_{lkg}$ respectively until t_4. Both currents transmit the power to the load.

Mode 4(t_3~t_4): After I_A meets zero crossing point at t_3 with a slope of $-(V_{C1}-V_{C2}/n)/L_{lkg}$, Mode 4 begins. Since the sign of I_A is negative and I_{lkg} is positive respectively in this mode, the power transfer is obtained only through the path of I_{lkg} with helps of the source energy and partial output energy stored in C_1. The reversed I_A provides ZVS conditions for Q_2.

Mode 5(t_4~t_5): When Q_4 is turned off at t_4, Mode 5 begins. After the junction capacitance of Q_2 and Q_4 discharges and charges respectively, the anti-parallel body diode of Q_2 is conducted with an initial current of $I_A(t_4)$ as shown in Fig. 3. At $t=t_5$, ZVS turn-on of Q_2 can be achieved and another half cycle will be begun.

2.2 Analysis of the Proposed Converter

2.2.1 Steady-state Analysis

Interval of Mode 3, D_2T, and average current of I_A and I_B can be simply obtained by calculating the area in a period as follows.

$$< I_A >= [\, D_2 - \frac{(1 - D - D_2)^2}{D_2} \,] \frac{I_I}{2} \tag{3}$$

$$< I_B >= [\, \frac{(1 - D)^2}{D_2} \,] \frac{I_I}{2n} \tag{4}$$

$$D_2 T = \frac{(1 - D)(1 + n)}{2n} T \tag{5}$$

From Fig. 3, the voltage-second balance equation can be derived as (6).

$$V_I DT = (V_{C1} - V_I)(1 - D)T \tag{6}$$

Voltage conversion ratio is obtained by using (1) through (6).

$$V_O = V_{C1} + V_{C2} = \frac{1}{1 - D} V_I + \frac{n}{1 - D} V_I = \frac{1 + n}{1 - D} V_I \tag{7}$$

2.2.2 ZVS Conditions

The ZVS condition of the main switches(Q_1 and Q_2) is dependent on the leakage inductance and the others(Q_3 and Q_4) use the boost inductors to achieve ZVS.

The ZVS condition of the main switches is expressed as,

$$\frac{1}{2} L_{lkg} I_A(t_4)^2 \geq \frac{2}{3} C_{OSS\_main} V_{C1}^{\ 2} + \frac{2}{3} C_{OSS\_aux} V_{C1}^{\ 2} \tag{8}$$

$$I_A(t_4) = \frac{n - 1}{2(1 - D)} \cdot \frac{V_O}{R_O} \tag{9}$$

As it is noted in (8) and (9), the leakage inductance supplies energy for charging C_{OSS_aux} and discharging C_{OSS_main}. ZVS of the main switches depends on the load conditions and leakage inductance.

The ZVS condition of the auxiliary switches is expressed as,

$$\frac{1}{2}L_{1,2}I_{L1,2}(t_1)^2 \geq \frac{2}{3}C_{OSS\_main}V_{C1}{}^2 + \frac{2}{3}C_{OSS\_aux}V_{C1}{}^2 \quad (10)$$

$$I_{L1,2}(t_1) = \frac{(n+1)}{2(1-D)} \cdot \frac{V_O}{R_O} \quad (11)$$

Since the boost inductors, L_1 and L_2, are large enough, ZVS of auxiliary switches is easily achieved. In other words, ZVS of auxiliary switches is always achieved if the main switches are turned on under ZVS conditions.

3. Experimental Results

The prototype of the proposed converter has been constructed with specifications as follows.

- V_I=42V, V_O=400V, I_{Omax}=1A,
- L_1=L_2=620μH, C_1=C_2=330μF/400V
- L_{lkg}=11μH, L_m=450μH, N1:N2(turn ratio)=14:42
- f_s (Switching frequency) =50kHz
- Q_1~Q_4 = FQA38N30(C_{oss}=670pF), D_1~D_4=FFPF20U40S

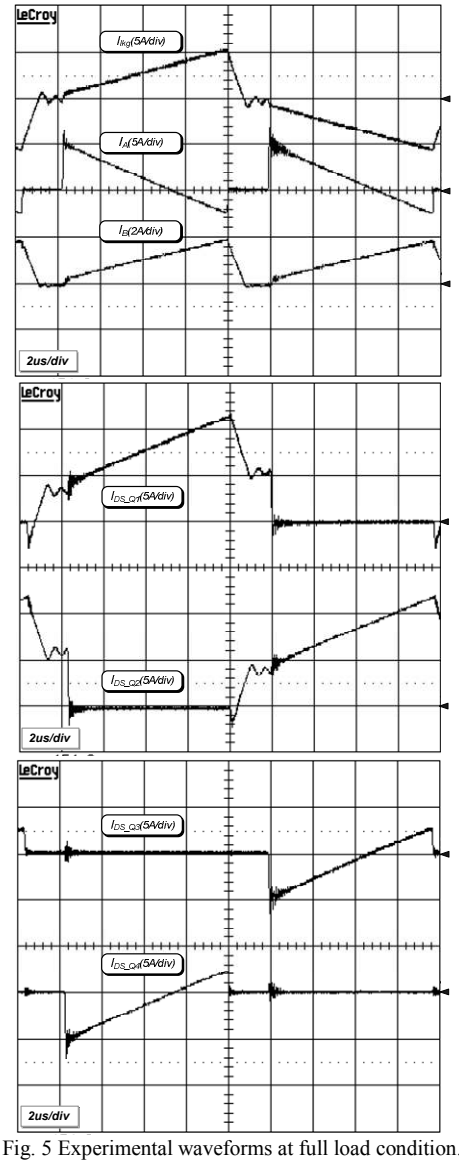


Fig. 5 Experimental waveforms at full load condition.

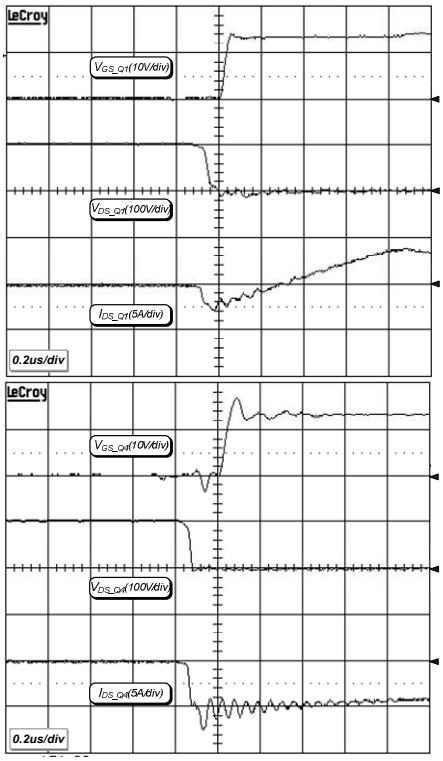


Fig. 6 Experimental ZVS waveforms at full load condition.

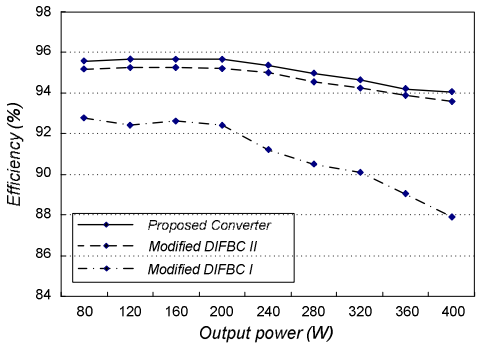


Fig. 7 Measured efficiency of the proposed converter.

It can be seen that all the waveforms agree well with the theoretical analysis in the previous section. With the values of leakage inductance and output junction capacitor used in the experiment, ZVS of all switches is achieved even below the 10% load condition. The proposed converter shows efficiency of 94.1% at full load conditions and the maximum efficiency is 95.7% near the half load conditions.

4. Conclusion

This paper presented the operational principle, analysis and experimental results of the proposed converter. The connected bidirectional parallel boost converter plays important roles such as powering to the load, clamping the voltage across the switches and making the current paths below half duty cycle. The proposed converter has higher voltage gain rather than conventional DIFBC. Furthermore, all of switches can be turned on under ZVS conditions in wide load ranges.

Reference

[1] Hyun-Wook Seong, "A New Non-isolated Boost Converter with Two-Inductor and One-transformer for Hybrid Electric Vehicle and Electric Vehicle ", KIPE Annual Conference 07, pp. 132-134, 2007, July.