Output Inductor Less Phase Shift Full Bridge Converter with Current Stress Reduction Technique for Server Power Application

Woo-Jin Lee*, Ki-Bum Park*, Tae-Won Heo**, and Gun-Woo Moon*

*Dept. of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology 373-1 Guseong-Dong, Yuseong-Gu, Daejeon, 305-701, Republic of Korea Phone: +82-42-869-3475, Fax: +82-42-861-3475

Email: gwmoon@ee.kaist.ac.kr
**Samsung Electro-Mechanics Co., LTD.

314, Maetan3-Dong, Yeongtong-Gu, Suwon, Gyunggi-Do, 443-743 Republic of Korea

Phone: +82-31-218-2911, Fax: +82-31-210-6322

E-mail: taewon.heo@samsung.com

Abstract

A new output inductor less phase shift full bridge converter with current reduction technique for server power application is proposed in this paper. The proposed converter can reduce the current stress by using the auxiliary circuit. Since the auxiliary circuit causes the additional resonance between the leakage inductor and auxiliary capacitor before the powering period, the proposed converter has lower current stress even no output filter inductor. Small size and circulating energy can be also the merits of the proposed converter. The operational principles and analysis are presented. Experimental results demonstrate that the current stress can be reduced effectively by using the auxiliary circuit without large output filter inductor.

1. Introduction

Recently, it is trend to design server power supply with server system infrastructure (SSI). The common way is that a boost converter as PFC stage rectifier the AC line to 380VDC or higher and the front-end dc-dc converter converts the 380VDC to 12VDC. After that, the dc-dc modules regulate 12VDC to whatever voltage needed.[1] Generally, since the input voltage of dc-dc modules is the same as the output voltage of PFC stage, one of characteristics in dc-dc modules can be the high input voltage. In addition, dc-dc modules for server power supply must supply the high output current. Thus, the secondary side of transformer in dc-dc modules not only should be simple structure with few components, but also operates symmetrically for the balanced voltage/current stress. Until now, several dc-dc converters, which can realize the high efficiency, small size, and high power density, have been proposed for the front-end dc-dc converter. Among them, one of good solutions is the phase shift full bridge (PSFB) converter which has been widely discussed to reduce component current/voltage stress and to provide the zero voltage switching (ZVS) operation of all power switches.[2-4] Generally, the output filter inductor is reasonable to reduce the current stress of both primary and secondary side of the

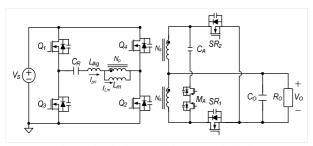


Fig. 1: Circuit diagram of the proposed circuit

transformer, because the front-end dc-dc converter with low output voltage and high output current is needed.[1] However, it also makes the large power loss, such as the core loss and conduction loss, bulky system, and increased cost. Moreover, the considerably large circulating energy is inevitable to achieve the ZVS operation. To avoid using the output filter inductor, another good solution is frequently the full bridge LLC resonant converter which shows many unique characteristics such as simple structure, excellent ZVS performance, and low voltage stress of primary power switches.[5-6] Even such good advantages, it still has some difficulties to apply to server power supply. This converter not only has a small magnetizing inductor, but also operates in the below resonance mode with the narrow powering period, in order to have a narrow variation of switching frequency.[5-6] This results in considerably higher current stress and lager conduction loss of both side of the transformer. Besides, the large output capacitance induced by the large current stress causes it to be bulky. To overcome above all problems effectively, we propose a new current stress reduction technique in PSFB converter without the output filter inductor for server power supply as shown in Fig. 1. The circuit diagram of proposed converter is very similar to those of the conventional PSFB converter with no output filter inductor except the auxiliary circuit. Since the output filter inductor doesn't exist in the proposed converter, the secondary side of the transformer is operating in discontinuous conduction mode (DCM). To reduce the current stress, the leakage inductor, L_{lkg} additionally resonates with the auxiliary capacitor, CA by controlling the auxiliary switches, MA after the commutation of SR₁ and SR₂ is finished. This results in both the primary and secondary current of the transformer is rapidly built up before powering. Therefore, although there is no output filter inductor, the current stress can be the almost same as that of conventional PSFB converter and much smaller than that of full bridge LLC resonant converter. In addition, the proposed converter has considerably smaller circulating energy compared with that of conventional PSFB converter. Thus, the proposed converter can be expected to eliminate the large output filter inductor effectively, to have small current stress and small circulating energy, and can realize the high power density, high performance and high efficiency.

2. OPERATIONAL PRINCIPLES

Fig. 2 shows the key waveforms of the proposed converter. The operation of the proposed converter can be divided into ten modes. One switching cycle of the proposed circuit is divided into two half cycles, t_0 - t_5 and t_5 - t_{10} . Since the operational principles of two half cycles are symmetric, only the first half cycle is explained. A half

cycle can be divided into 5 modes and its equivalent circuits are shown in Fig. 3. The switches of leading leg (Q_1 and Q_3) and lagging leg (Q_2 and Q_4) are turned on and off alternately with the constant duty ratio. The phase difference between both legs determines the operational duty cycle of the converter, where $D_{\text{eff}}T_s$ is the operational conduction time and $D_{\text{free}}T_s$ is the phase shifted time. To illustrate the steady state operation, two assumptions are made as follow:

- The power switches such as Q_1 , Q_2 , Q_3 , Q_4 , SR_1 , SR_2 , and M_A are ideal except for their internal diodes and output capacitors, C_{oss} .
- The output voltage V_o is constant during a switching period.

Mode 1 ($t_0 \sim t_1$): After the ZVS of Q_2 is achieved and the auxiliary switch, M_A is turned on, Mode 1 begins. During this mode, since the leakage inductor, L_{lkg} is resonated with the auxiliary capacitor, C_A , the primary current, I_{pri} is increased rapidly. Concurrently, the secondary current, which flows through the auxiliary circuit, is also increased rapidly during very short time. Thus, during mode 1, the primary current can be expressed as follows:

$$I_{pri}(t) = V_S \sqrt{\frac{n^2 C_A}{L_{lkg}}} \sin \omega_r(t - t_0) + I_{Lm}(t_0), \qquad (1)$$

where, $\omega_r = 1/n\sqrt{L_{lkg}C_A}$.

Mode 2 ($t_1 \sim t_2$): After SR_1 is turned on, mode 2 begins. Since SR_1 is turned on, the power is transferred to output. During this mode, both the primary and magnetizing current can be expressed as follows:

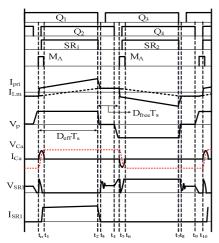


Fig. 2: Key waveforms of proposed converter

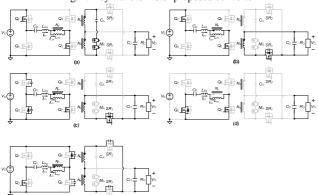


Fig. 3: Equivalent circuits of proposed converter, (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4 (e) Mode 5

$$I_{pri}(t) = V_S \sqrt{\frac{n^2 C_A}{L_{lkg}}} + \frac{V_S - V_O/n}{L_{lkg}} (t - t_0) + I_{Lm}(t_0) .$$
 (2)

$$I_{Lm}(t) = \frac{Vo/n}{L_m}(t - t_0) + I_{Lm}(t_0).$$
(3)

In this case, SR_1 is turned on at the quarter period of the resonant period which is induced by L_{lkg} and C_A . Since the current which flows through the auxiliary circuit, can be a half sinusoidal waveform, the auxiliary switch, M_A can be turned off at half resonant period.

Mode 3 ($t_2\sim t_3$): After Q_1 is turned off, the primary current, I_{pri} starts to charge and discharge the output capacitors of Q_1 and Q_3 respectively. When the voltage across Q_3 becomes 0V, I_{pri} begins to flow through the internal diode of Q_3 . Concurrently, the voltage across the transformer primary side V_p , is decreased to 0V and the voltage across L_{lkg} , is also decreased. Thus, the primary current is decreased with the slope of $-V_0/nL_{lkg}$. When the primary current is the same as the magnetizing current, mode 3 is finished.

Mode 4 (t_3 ~ t_4): After the primary current is the same as the magnetizing current, the mode 4 begins. When the primary current, I_{pri} is smaller than the magnetizing current I_{Lm} , SR_1 is turned off. After that, the secondary side of transformer can be regarded as the open circuit. Thus, the freewheeling current of primary side is the same as the magnetizing current. At the same time, since the voltage across the primary side of transformer is equal to 0V, both the primary and magnetizing current is maintained to be the value before. During this mode, the ZVS of Q_3 can be achieved.

Mode 5 ($t_4\sim t_5$): After the Q_2 is turned off, Mode 5 begins. During this mode, the magnetizing current starts to charge and discharge the output capacitors of Q_2 and Q_4 respectively. Thus the proper dead time is needed for the ZVS operation of lagging leg switches.

The circuit operation of $t_5 \sim t_{10}$ is similar to that of $t_0 \sim t_5$. Subsequently, the operation from t_0 to t_{10} is repeated.

3. ANALYSIS & DESIGN CONSIDERATIONS

Fig. 4 (a) shows the equivalent circuit when the auxiliary circuit is operating. From this figure, the resonant current which is induced by the resonance between the leakage inductor and auxiliary capacitor can be obtained as follows:

$$I_{pri}(t) = V_S \sqrt{\frac{n^2 C_A}{L_{lkg}}} \sin \omega_r t . \tag{4}$$

To obtain the DC conversion ratio, we assume that one switching period can be divided into two periods such as $D_{eff}T_s$ and $D_{free}T_s$. In addition, the period $D_{eff}T_s$ starts at the quarter resonant period so as to the secondary current can be increased from the peak value of resonant current as shown in Fig. 4 (b). From the above assumptions and the equation (4), the secondary current can be expressed as follows:

$$I_{\text{sec}}(t) = \frac{V_S}{n} \sqrt{\frac{n^2 C_A}{L_{lkg}}} + \frac{V_S - V_O / n}{n L_{lkg}} t . \tag{5}$$

Therefore, the output current, I_0 which is the same as the average value of secondary current can be expressed as follows:

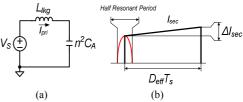


Fig. 4: Figure for analysis, (a) Equivalent circuit (b) Simple current waveform

Woo-Jin Lee, Ki-Bum Park, Tae-Won Heo, and Gun-Woo

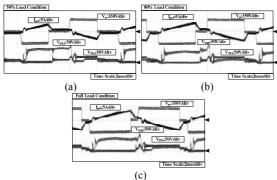


Fig. 5: Experimental waveforms, (a) 50% load condition (b) 80% load condition (c) full load condition

$$Io = \frac{Vo}{Ro} = \frac{Vs}{n} \sqrt{\frac{n^2 C_A}{L_{lkg}}} D_{eff} T_s + \frac{1}{2} \frac{Vs - Vo/n}{n L_{lkg}} D_{eff} T_s . \tag{6}$$

From the equation (6), we can obtain the DC conversion ratio as follows:

$$\frac{V_O}{V_S} = n \frac{1 + \frac{2}{D_{eff}T_s} \sqrt{C_A L_{lkg}}}{1 + \frac{2n^2 L_{lkg}}{(D_{eff}T_s)^2 R_O}} \,. \tag{7}$$

From the equation (7), the turn ratio of transformer can be hardly obtained. The auxiliary capacitance, C_A is can be obtained as follow:

$$C_A = L_{lkg} \left[\frac{V_O}{V_S} \frac{1}{D_{eff} T_s R_O} - \frac{D_{eff} T_S \left(V_S - V_O / n \right)}{2n L_{lkg} V_S} \right]^2. \tag{8}$$

4. EXPERIMENTAL RESULTS

A 700W prototype of the proposed converter has been built for the experiment. Fig. 5 shows the experimental waveforms at 50%, 80%, and full load. As can be seen in Fig. 5, since the leakage inductor is resonated with the auxiliary capacitor, the primary current is increased rapidly before the powering period. This results in less current stress in each component. On the other hand, as the load goes to light load, the variation of operating duty is getting wide compared to that in case of conventional PSFB converter. This is because the secondary side of proposed converter is operating in DCM. In addition, before the powering period the leakage inductor is always resonated with the auxiliary capacitor as long as the auxiliary circuit operates. Thus, even though the load is light load, both the primary and secondary current is rapidly increased as much as in case of full load. This makes the power loss in the auxiliary circuit be constant in any condition. Therefore, the proposed converter shows the lower efficiency at the light load. However, the proposed converter shows the higher efficiency than that of converter PSFB converter in heavy load. This is because the proposed converter shows the lower current stress in each component.

5. CONCLUSIONS

A new output inductor less PSFB converter for server power application is proposed in this paper. The large output filter inductor is eliminated in the proposed converter so as to reduce the core loss and conduction loss as well as the size. However, the current stress in both the primary and secondary side is increased because of the lack of output filter inductor. In the proposed converter, the resonance between the leakage inductor and auxiliary capacitor makes the current stress reduced as much as that of conventional PSFB converter. Before the powering period, the leakage inductor is resonated with the auxiliary capacitor with the operation of auxiliary

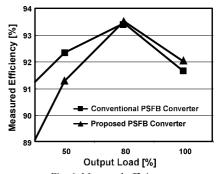


Fig. 6: Measured efficiency

circuit. This causes both the primary and secondary current to be increased rapidly. Thereby, the increase of current stress shows some limitations during the powering period. A prototype has been experimented to prove the validity of the proposed converter. On the other hand, the proposed converter has the narrow operating duty at light load compared to that of conventional PSFB converter. This is because the secondary side of proposed converter is operating in DCM. Additionally, as long as the auxiliary circuit operates, the leakage inductor is always resonated with the auxiliary capacitor before the powering period. Thus, the variation of operating duty is getting wide according to load variations. Therefore, the efficiency of proposed converter is lower than that of conventional PSFB converter at light load. However, in heavy load, the proposed converter shows the higher efficiency because of the lower current stress. Therefore, the proposed converter demonstrates its suitability as a dc-dc module for server power supply owing to its small size, low cost, and high efficiency.

REFERENCES

- Dong Li; Xinbo Ruan, "Comparison of Three Front-end DC-DC Converters for 1200W Server Power Supply", *Power Electronics Specialists*, IEEE 36th Conference on, Sept 2005, pp394-398.
- [2] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switching PWM converter," in *IEEE-APEC Conf. Rec.*, 1990, pp. 275-284.
- [3] R. Redl, N. O. Sokal, and L. Balogh, "A novel soft-switching full-bridge dc/dc converter: Analysis, design considerations, and experimental results at 1.5kW, 100kHz," *IEEE Trans. Power Electron.*, vol. 6, pp. 408-418, July 1991.
- [4] R. Redl, L. Balogh, and D. W. Edwards, "Optimum ZVS full-bridge dc/dc converter with PWM phase-shift control: Analysis, design considerations, and experimentation," in IEEE-APEC Conf. Rec., 1994, pp. 159-165.
- [5] Bo Yang; Lee, F. C.; Zhang, A. J.; Guisong Huang, "LLC resonant converter for front end DC/DC conversion," *Applied Power Electronics Conference and Exposition*, 2002. APEC 2002. Seventeenth Annual IEEE, Volume: 2, 2002 Page(s): 1108-1112 vol.2.
- [6] Lazar, J. F.; Martinelli, R., "Steady-state analysis of the LLC series resonant converter" Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE, Volume: 2, 2001 Page(s): 728-735 vol.2.