Output inductor-less active clamp forward converter employing current boost-up circuit for high power density adaptor

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Abstract

This paper proposes an output inductor-less active clamp forward converter employing current boost-up circuit for high power density adaptor. By applying the proposed current boost-up circuit, the proposed converter has low conduction loss and low voltage ringing of the secondary rectifier. This paper presents the analysis of the proposed converter and a comparison between the proposed converter and the conventional converter through experiment

1. INTRODUCTION

Recently, many isolated DC-DC converter topologies suitable for high power density and high current applications have been presented [1]~[3]. All of them try to reduce size and cost by optimizing the magnetic component and minimizing the number of passive components. The conventional active clamp forward converter without output inductor can be considered for high power density [3]. However the conventional converter has high peak current, which causes the serious heat problem at the secondary side due to high conduction loss. Therefore the conventional converter is undesirable for high current applications. To overcome this problem, the proposed converter adopts a current boost up circuit across the output diode. A current boost up circuit decreases rms value of the transformer secondary current and clamps the rectifier voltage ringing. These features make the proposed converter suitable for high power density, and high current applications.

In the following sections, the detailed analysis of the proposed converter will be presented. Experiment results demonstrate that merits and demerits of the proposed circuit.

2. OPERATION PRINCIPLE

Fig.1 shows the proposed current boost up active-clamped forward without output filter is shown in Fig.1.

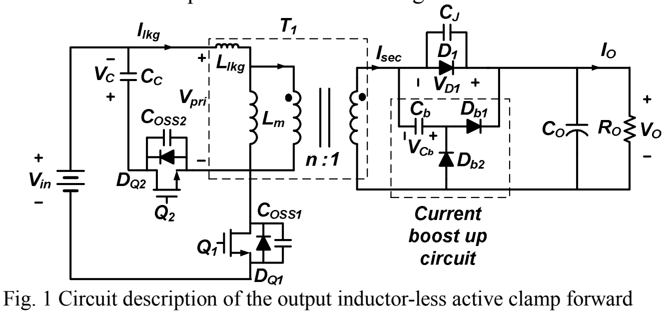


Fig. 1 Circuit description of the output inductor-less active clamp forward converter employing current boost up circuit.

According to the characteristics of the forward converter, step-down operation, the output voltage V_O reflected to the transformer primary side, V_{pri}, should be lower than the input voltage V_{in}.

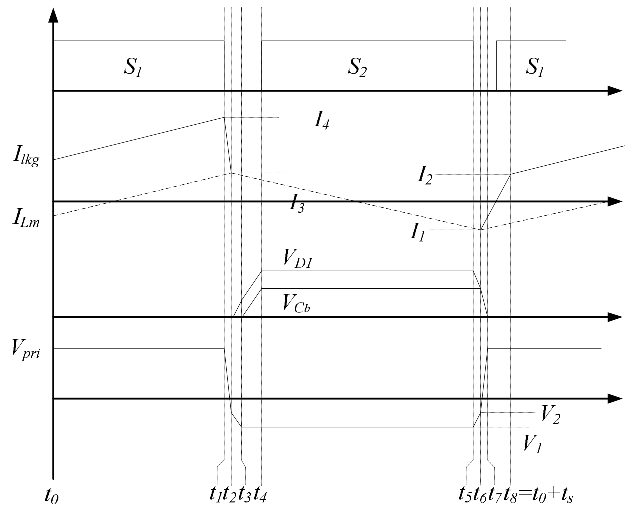


Fig. 2 Key waveforms of the proposed converter

Key waveforms of the proposed converter in a switching period are shown in Fig.2. As can be seen, each switching period can be subdivided into eight modes described in the following.

Mode 1 (t_0 –t_1): This mode begins at t_o when Q_1 is turned-on. This interval represents the powering mode, the energy is transferred to the output from the source. V_{in} is applied to the primary winding of transformer T_1, it makes I_{lkg} linearly increase. I_4 is the maximum value of I_{lkg}.

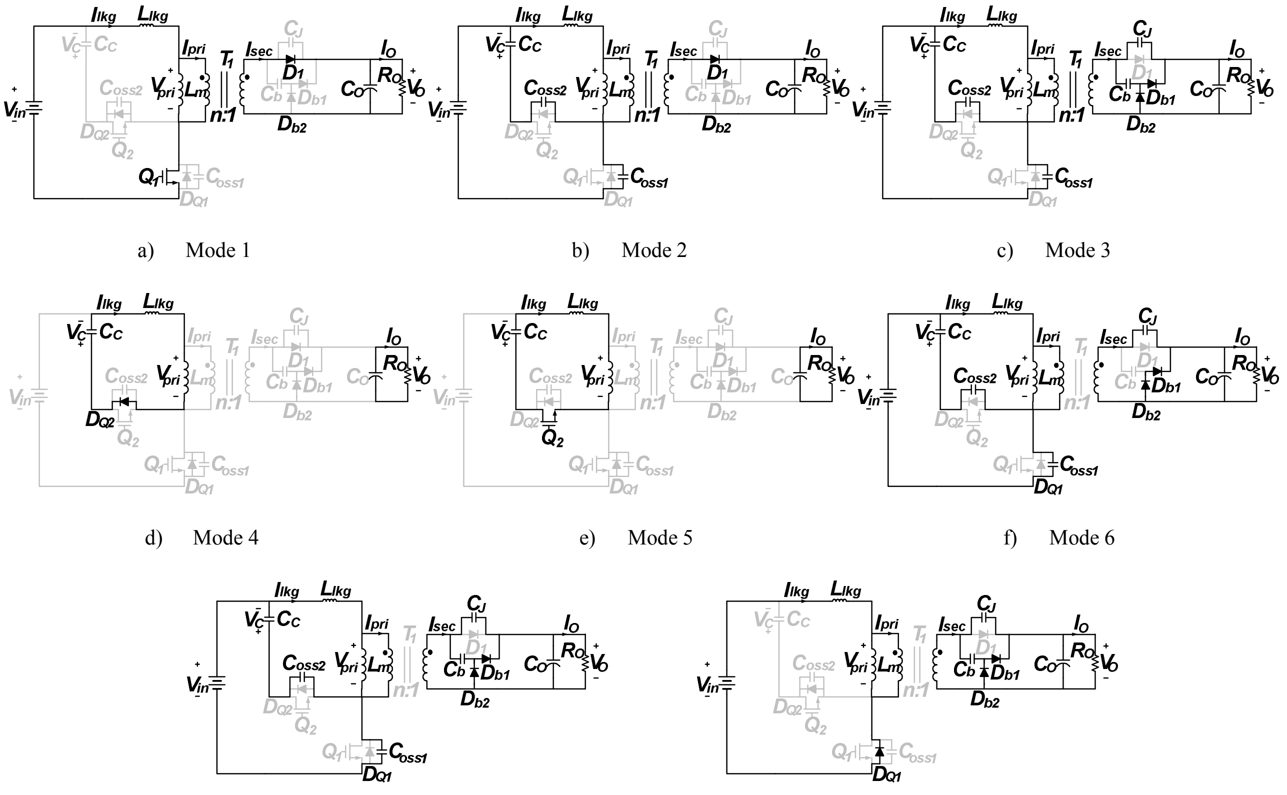
$$I_{lkg}(t)=\frac{V_{in}-V_{pri}}{L_{lkg}}t+I(t_0) \tag{1}$$

$$I_4=\frac{V_{in}-V_{pri}}{L_{lkg}}DT_S+I_2 \tag{2}$$

Where D is duty ratio of the switch Q_1 and T_S is the switching period.

Mode 2 (t_1 –t_2): Mode 2 begins at t_1 when Q_1 is turned-off. At the same time, a resonance between L_{lkg}, C_{oss1}, and C_{oss2} is started. In this mode, D_{b1} is reverse biased, and D_{b2} is forward biased. At the end of this mode, the value of I_{Lm} equals that of $I_{lkg} = I_3$.

$$I_3 = I_1+\frac{n\times V_O}{L_m}DT_S \tag{3}$$



a) Mode 1 b) Mode 2 c) Mode 3

d) Mode 4 e) Mode 5 f) Mode 6

g) Mode 7 h) Mode 8

Fig 3. Equivalent circuit of the proposed converter

$$I_{lkg}(t) = I_4 \cos\left(\sqrt{\frac{1}{2L_{lkg}C_{OSS}}}\,t\right) \tag{4}$$

Where $C_{OSS} = C_{OSS1} = C_{OSS2}$.

Mode 3 (t_2 – t_3): At t_2, D_1 is reverse biased. During this mode L_m and L_{lkg} resonate with C_{oss1}, C_{oss2}, C_J and C_b. At the end of this mode, the voltage across Q_2 is 0 and the body diode of Q_2, D_{Q2}, is forward biased.

$$V_1 = \frac{V_C}{n} \tag{5}$$

Mode 4 (t_3 – t_4): D_{Q2} is still forward biased. This mode is the freewheeling mode.

Mode 5 (t_4 – t_5): Since Q_2 is turned on before I_{lkg} decreases to zero the ZVS operation of Q_2 is guaranteed regardless of load variations. In heavy and medium load condition, the ZVS operation of Q_2 can be easily achieved due to large leakage-inductor current at t_1. The value of V_C is increased by I_{lkg}. V_{pri} is equal to V_C. The current of the magnetizing inductor is decreased linearly as follows:

$$I_{Lm}(t) = I_3 - \frac{nV_O}{L_m}t \tag{6}$$

From Fig. 1, the ZVS condition of Q_2 can be expressed as follows:

$$\frac{1}{2}L_{lkg}I_4^2 \geq \frac{1}{2}(2C_{OSS})(V_{in}+V_C)^2 + \frac{1}{2}C_b\left(\frac{V_C}{n}\right)^2 \tag{7}$$

Mode 6 (t_5 – t_6): At t_5, Q_2 is turned-off. L_m and L_{lkg} resonate with C_{oss1}, C_{oss2} and C_J. In this mode, D_{b1} is turned-on, and Db2 is turned-off. Both of C_{oss1} and C_J are discharged, C_{oss2} is charged.

Mode 7 (t_6 – t_7): In this mode, I_{pri} is boost up by discharging C_b. At the end of mode 7, D_{Q1} is forward biased, and the resonance between L_m, L_{lkg}, C_{oss1}, C_{oss2}, C_J, C_b is ended. The boost-up current ($I_2 - I_1$) is decided as follows:

$$I_{lkg}(t) = (|I_2| + |I_1|)\sin\left(\sqrt{\frac{1}{L_{lkg}(2C_{OSS}+C_b)}}\,t\right) \tag{8}$$

Mode 8 (t_7 – t_8): This mode is similar to mode 4, except D_{Q1} is forward biased. By turning on Q_1 during the value of I_{lkg} is negative, Q_1 can achieve ZVS.

$$\frac{1}{2}L_{lkg}I_1^2 \geq \frac{1}{2}(2C_{OSS})(V_{in}+V_C)^2 + \frac{1}{2}C_b\left(\frac{V_C}{n}\right)^2 \tag{9}$$

3. Design considerations

In this section, the large signal modeling is presented to obtain DC conversion ratio.

For the convenience of the analysis of the steady state operation, several assumptions are made as follows:

a) Interval from t_1 to t_4 and interval from t_5 to t_8 are neglect.
b) V_C, V_O is constant.
c) The secondary leakage inductance: L_{lkg}/n^2.
d) $C_b >> C_{OSS}$.

According to these assumptions, the switching period can be divided into only two modes. The average current of I_{sec}, the difference between I_{lkg} and I_{Lm}, is equal to I_O. In Fig. 2, we can analyze boosting current, $I_2 - I_1$, by calculating following equation (8), and (9)

$$L_{lkg}(I_2 - I_1)^2 = \frac{1}{2}C_b \times \left(\frac{V_C}{2}\right)^2 + C_{OSS}{}^2 \times \left(\frac{V_{in}+V_C}{2}\right)^2 \tag{10}$$

$$V_C = \frac{D}{1-D} V_{in} \tag{11}$$

Substituting (3) into (2) gives the following expression for $I_2 - I_1$:

$$I_2 - I_1 = \frac{V_{in}}{2(1-D)} \sqrt{\frac{1}{2L_{lkg}} \left(C_b D^2 + 2C_{OSS}\right)} \tag{12}$$

$$\frac{V_O}{R} \times T_S = \frac{1}{2}\left(I_2 - I_1 + I_4 - I_3\right) D \times T_S \tag{13}$$

From (2) and (3), $I_4 - I_3$ can be expressed as follows:

$$I_4 - I_3 = I_2 + \frac{V_{in} - n \times V_O}{L_{lkg}} DT_S - \left(I_1 + \frac{n \times V_O}{L_m} DT_S\right) \tag{14}$$

From (4), (5) and (6), an expression for the voltage conversion ratio can be derived as follows:

$$G = \frac{R_O L_m D\left[\sqrt{2L_{lkg} C_b} + 2(1-D)T_S\right]}{2(1-D)\left(2L_{lkg} L_m + R_O L_m nDT_S + R_O L_{lkg} nDT_S\right)} \tag{15}$$

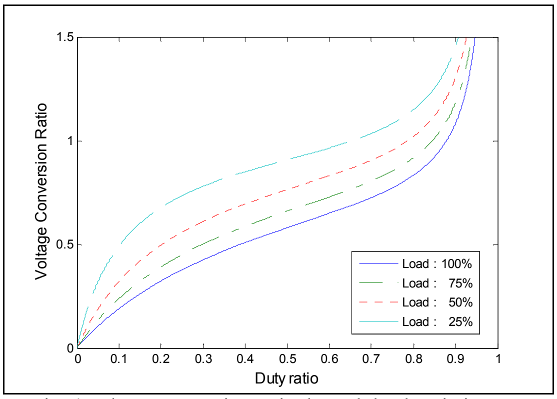


Fig. 4 Voltage conversion ratio through load variation

Fig. 4 shows the voltage conversion ratio according to the load variation. Since the proposed converter has active clamp circuit, the voltage stress of switches gets higher as the duty ratio gets larger. Therefore the ZVS condition of the switch is poor. In case of the small duty ratio, although the variation of the duty ratio is small by load condition, rms value of the secondary current of the transformer is high. Therefore the duty ratio can be designed by considering the ZVS condition, the secondary conduction loss of the transformer and the variation of the duty ratio.

4. Experiment Results

Based on the analysis of the proposed converter, a prototype circuit has been built. The specification of the prototype follows:

a) Input voltage V_{in} : $90V_{ac}$
b) Output voltage V_o : 14.5V
c) Maximum output power P_o : 45W
d) Switching frequency f_s : 100kHz
e) Turn ratio of the transformer n : 8.4

Table 1 shows components are used for the prototype of the 14.5V, 45W converter operated at 100kHz has been built. The transformer was built on a PC44PQ2016 core ($N_p = 42$, $N_s = 5$).

Switching frequency (f_s)	100kHz
Switches (Q_1,Q_2)	FQP20N60C3
Diode (D_1)	V60100C
Turn ratio (N_p:N_s)	42 : 5
Leakage inductance (L_{lkg})	12uH
Magnetizing inductance (L_m)	1.5mH
Boost capacitor (C_b)	80nF

Table. 1 Component lists for the prototype converter

Fig. 5 shows key waveforms of the proposed converter. The primary current I_{lkg} and the voltage across the primary side of the transformer, Vpri, are well agreed with the theoretical analysis. We can see the primary current I_{lkg} is boosted.

Fig. 6 shows the efficiency of the proposed converter and that of the conventional active-clamped forward converter without output filter, by changing load current. As shown in this figure, the efficiency of the proposed converter is about 0.7% higher than that of the conventional one at heavy load range.

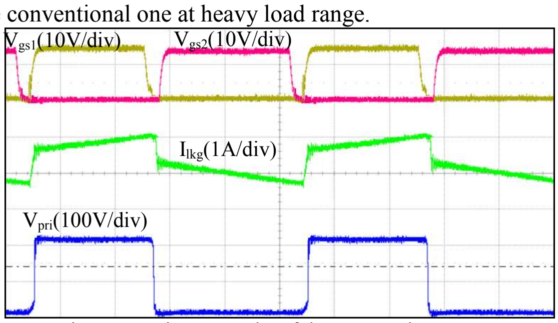


Fig. 5 Experiment results of the proposed converter (2us/div)

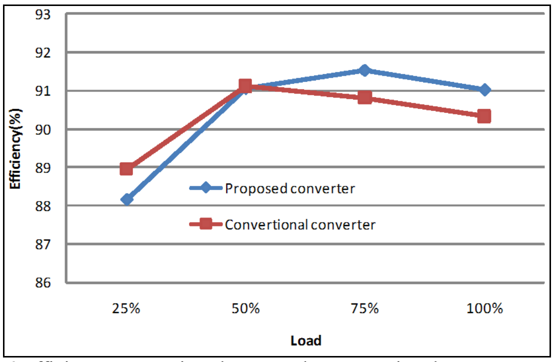


Fig. 6 Efficiency comparison between the conventional converter and the proposed converter

5. Conclusion

In this paper, an output inductor-less active clamp forward converter employing current boost-up circuit for high power density is presented. The proposed converter has low conduction loss by applying boost up circuit. An operation principle and a simplified analysis of the proposed converter are given. The experimental result shows that the efficiency of the proposed converter is 0.7% higher than that of the conventional one. Therefore, the proposed converter is suitable for high power density and high current applications.

Reference

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