

# Interleaved Forward Converter for High Input Voltage Application with Common Active-Clamp Circuit

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## Abstract

A new interleaved forward converter, adopting series-input parallel-output structure with a common transformer reset circuit, is proposed in this paper. Series-input structure distributes the voltage stress on switches, which makes it suitable for high input voltage application. Paralleling output stage with an interleaving technique enables the circuit handle large output current and reduces filter size. In addition, since two forward converters share one active-clamp circuit for the transformer reset, its primary structure is simplified. All these features make the proposed converter promising for high input voltage applications with high efficiency and simple structure.

## 1. Introduction

Till now, various isolated converters have been developed [1]. Among them, a forward converter, which is derived from a buck converter, is one of the most well-known circuits in low-to-medium power step-down applications due to its simplicity and high efficiency [2]-[3]. In spite of its popularity, designing a forward converter requires many tradeoffs relating with switch current/voltage stresses and transformer reset schemes to accommodate various applications.

The galvanic isolation of forward converter costs an additional transformer reset circuit such as a tertiary winding, a RCD-clamp circuit, and an active-clamp circuit (ACC) [2]-[3]. The current/voltage stress on device, circuit complexity, and efficiency are varied according to these different reset schemes. In general, as the operating duty cycle is increased, the voltage stress on switch is increased to ensure the transformer reset, though the current stress on switches is reduced. The typical voltage stress on switch may exceed twice the input voltage with about half duty cycle. This fact makes the forward converter not suitable for high input voltage applications such as a front-end converter of which the input voltage is about 400-Vdc. In this case, the usage of high voltage rating switch, which features low performance and high cost, is inevitable. Although relative low voltage stress can be achieved by selecting small duty cycle, the current stress on switch and the output filter size would be increased to the contrary.

On the other hand, the interleaving technique for paralleling converter power stage is a useful approach that is often used in high-power applications to achieve distributed device stress and reduce an output filter size [4]. As shown in Fig. 1, the parallel connected interleaved forward (IF) converter is one of the issues [5]. Although IF converter is attractive for its high power capability, high voltage stress on switch is still a heavy burden in high input voltage applications. Moreover, each forward converter needs its own transformer reset circuit which increases circuit complexity and fair current sharing between modules needs careful design of power stage and/or additional control.

To relieve the above-mentioned limitations, a new IF converter, that is suitable for high input voltage applications with simple

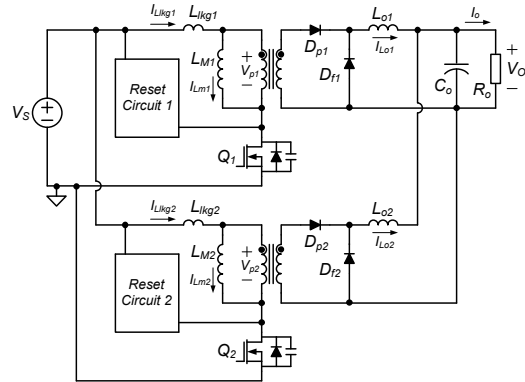


Fig. 1 Conventional IF converter.

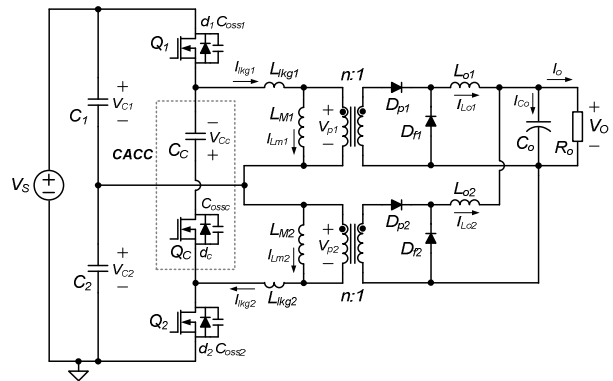


Fig. 2 Proposed IF converter with CACC.

structure, is proposed in this paper as shown in Fig. 2. By adopting the series-input structure, the voltage stresses on switches are distributed resulting in the usage of low-voltage rated switch, and the parallel-output structure with the interleaving control enables high output current capability with distributed current stress and reduced output filter size. Moreover, it is remarkable that two forward converters share one common ACC (CACC), for the transformer reset and zero-voltage switching (ZVS) of switches, resulting in the simplified circuit.

## 2. Operational Principle

The basic operation of proposed converter is an interleaved operation between two active-clamp forward (ACF) converters with CACC. Since two ACF converters operate symmetrically,  $V_{C1}$  and  $V_{C2}$  have same voltage, i.e.,  $V_s/2$ . For the price of removing one ACC, one of the main switches cooperates with the auxiliary switch  $Q_c$  by turns in each transformer reset action. That is, for the proper transformer reset of one module, the main switch of the other module should be on-state to form the conducting path for the transformer magnetizing current. As a result, the desired operation of each ACF converter is obtained above 0.5 duty cycle. Therefore, the operation principle of proposed converter is divided

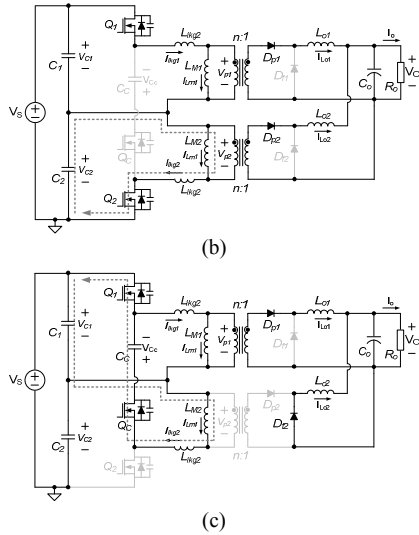
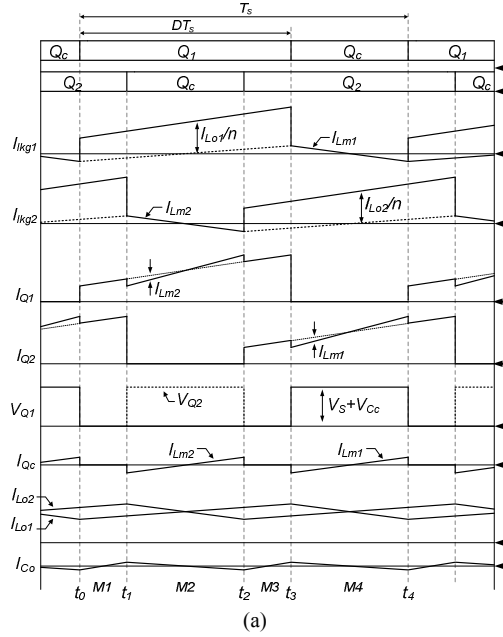


Fig. 3 Above 0.5 duty cycle operation. (a) Key waveforms. (b) Topological state of M1. (c) Topological state of M2.

into two regions, i.e., above 0.5 duty cycle and below 0.5 duty cycle, as follows.

### 2.1. Above 0.5 duty cycle operation ( $D > 0.5$ )

The key waveforms and topological states are presented in Fig. 3. The main switches  $Q_1$  and  $Q_2$  are switched with half-period phase difference for the interleaved operation, and each main switch and  $Q_C$  are switched complementary for the transformer reset and ZVS of switches. The mode analysis is focused on the distinct magnetizing current path and transient period is ignored. In Figs. 3(b) and 3(c), only the magnetizing current  $I_{Lm2}$  is marked by the dotted line to explain the transformer reset operation.

During the interval  $t_0 \sim t_1$ , both  $Q_1$  and  $Q_2$  conduct.  $V_S/2$  is applied to each transformer, thus both module transfer the power from the input to the output as shown in Fig. 3(b).  $I_{Lm1}$  and  $I_{Lm2}$  increase linearly and  $V_{QC}$  is limited by  $V_S+V_{Cc}$ . At  $t_1$ ,  $Q_1$  is turned off and the lower side output inductor current  $I_{L02}$  starts to freewheel. Since  $Q_1$  is still conducting,  $I_{Lm2}$  flows through  $Q_C$ ,  $C_C$ ,  $Q_1$ , and  $C_1$  as depicted by the dotted line of Fig. 3(c). Therefore,  $V_S/2+V_{Cc}$  is applied reversely to the lower side transformer and  $I_{Lm2}$  decreases linearly.  $I_{Q1}$  comprises  $I_{Lkq1}$  and  $I_{Lm2}$ , and  $V_{Q2}$  is

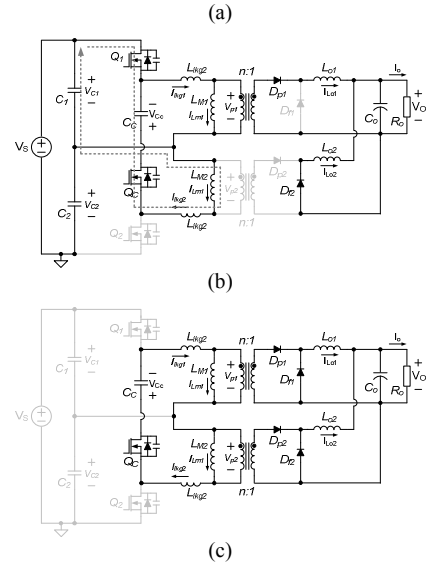
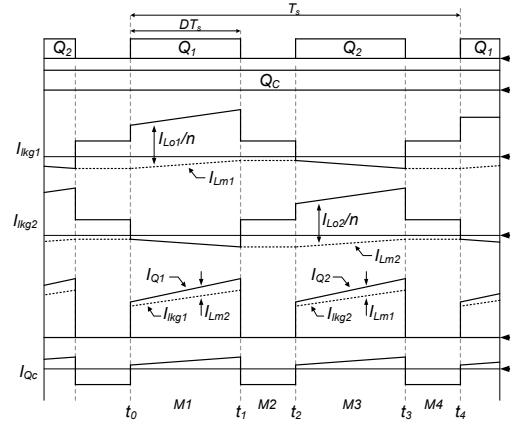


Fig. 4 Below 0.5 duty cycle operation. (a) Key waveforms. (b) Topological state of M1. (c) Topological state of M2

limited by  $V_S+V_{Cc}$ . The interval  $t_2 \sim t_4$  is symmetrical to  $t_0 \sim t_2$ .

From the volt-sec. balance across  $L_{M1}$  and  $L_{M2}$ ,  $V_{Cc}$  is obtained as (1). It is noted that the voltage stress of all switches is expressed as (2), which is half of that of conventional ACF converter.

$$V_{Cc} = \frac{2D-1}{2(1-D)} V_S \quad (1)$$

$$V_Q = \frac{1}{2(1-D)} V_S \quad (2)$$

### 2.2. Below 0.5 duty cycle operation ( $D < 0.5$ )

The gate signal for  $Q_C$  is 'OR' signal between the inverted gate of main switches, therefore  $Q_C$  is always on-state below half duty cycle region. That is,  $Q_C$  is shorted and only the main switches are operated in interleaving way as shown in Fig. 4(a). In this region,  $V_{Cc}$  becomes 0-V by the volt-sec. balance across transformer, and the transformer magnetizing currents have a negative offset with respect to the reference direction.

During the interval  $t_0 \sim t_1$ , only  $Q_1$  conducts and the power is transferred to output through the upper module.  $I_{Lm1}$  has negative offset, hence the difference between  $I_{L01}/n$  and  $I_{Lm1}$  flows through  $L_{Lkq1}$ . Since  $Q_2$  is off-state,  $I_{Lm2}$  flows through  $Q_1$  as depicted in the dotted line of Fig. 4(b), therefore  $I_{Q1}$  contains  $I_{Lm2}$  as well as  $I_{Lkq1}$ . At  $t_1$ ,  $Q_1$  is turned off. Since both  $Q_1$  and  $Q_2$  are off-state,  $I_{Lkq1}$  and  $I_{Lkq2}$  flows through  $C_C$  having the same current. Both two transformers are shorted and both  $I_{L01}$  and  $I_{L02}$  freewheel. The interval  $t_2 \sim t_4$  is symmetrical to  $t_0 \sim t_2$ .

Using the current-sec. balance of  $C_C$ , the offset of  $I_{Lm1}$  and  $I_{Lm2}$  can be expressed as (3). Because  $V_{Cc}$  is zero and  $Q_C$  is shorted, the voltage stress on main switch is  $V_S$ .

$$I_{Lm\_offset} = \frac{(0.5 - D)}{4n(1 + D)} I_o \quad (3)$$

### 2.3. Design consideration

Below 0.5 duty cycle region, the main switches are under hard-switching condition and  $I_{Lm1,2}$  has offset, that is, ACF converter loses its own characteristics. Therefore the above 0.5 duty cycle region is preferred for the nominal operation. However, high voltage stress on switch, which is increased as the duty cycle increase, can be more severe problem in this region. Therefore, the nominal duty cycle should be chosen as possible as small to reduce the voltage stress, but should be still above 0.5. The below 0.5 duty cycle region can be used for the regulation in discontinuous conduction mode (DCM) and for the soft start-up.

## 3. Simulation Results

To verify the validity of proposed converter, a 300-W converter prototype with 320~390-Vdc input and 48-Vdc output operating at 100-kHz has been built. To utilize 600-V switch with 10% margin, the nominal duty cycle at the maximum input voltage 390-Vdc is selected at about 0.55. The proposed converter has the following parameters: transformer turn ratio  $n=38/18$ , transformer magnetizing inductance  $L_{M1}=L_{M2}=1.5\text{mH}$ , transformer leakage inductance  $L_{lk1}, L_{lk2}=7\text{uH}$ , output inductors  $L_{o1}=L_{o2}=150\text{uH}$ ,

Fig. 5 shows the key simulation waveforms of  $D>0.5$  operation. The entire waveforms are agreed well with theoretical analysis. It can be observed that  $I_{Lm1}$  and  $I_{Lm2}$  flow through  $I_{Q2}$  and  $I_{Q1}$ , respectively, during the transformer reset action. In case of that  $V_S=385\text{-Vdc}$ , the voltage stress on switch is about 440-V as shown in Fig. 5(a), and in case of that  $V_S=320\text{-Vdc}$ , the voltage stress reaches up to 510-Vdc as shown in Fig. 5(b). Fig. 6 presents the operation in  $D<0.5$  operation, where the voltage stress on switch is clamped to  $V_S$ , i.e., 385-Vdc.

## 4. Conclusions

IF converter is one of the attractive approaches in high power applications for its distributed devices stress and small filter size. However, high voltage stress on switch is heavy burden in high input voltage applications. Moreover, each forward converter needs its own transformer reset circuit. To relieve these problems, a new IF converter, that is suitable for high input voltage applications with simple structure, is proposed. By adopting the series-input structure, the voltage stresses on switches are distributed while the parallel-output structure enables the high output current capability. Moreover, two forward converters share one common ACC, its structure is simplified. Therefore, the proposed converter is promising for high input voltage applications with high efficiency, low cost, and simple structure.

## Reference

- [1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power electronics*, 2<sup>nd</sup> Ed., John Wiley, New York, USA, 1950, pp. 39-55.
- [2] F. D. Tan, "The forward converter: from the classic to the contemporary," in *Proc. IEEE APEC*, 2002, pp. 857-863.
- [3] A. Acik and I. Cadirci, "Active clamped ZVS forward converter with soft-switched synchronous rectifier for high efficiency, low output voltage applications," in *Proc. IEE Electr. Power Appl.*, vol. 150, no. 2, pp. 165-175, Mar., 2003.
- [4] B. A. Miwa, D. M. Otten, and M. F. Schlecht, "High efficiency power factor correction using interleaving techniques," in *Proc. IEEE. APEC*, 1992, pp. 557-568.
- [5] M. T. Zhang, M. M. Jovanovic, and F. C. Lee, "Analysis and

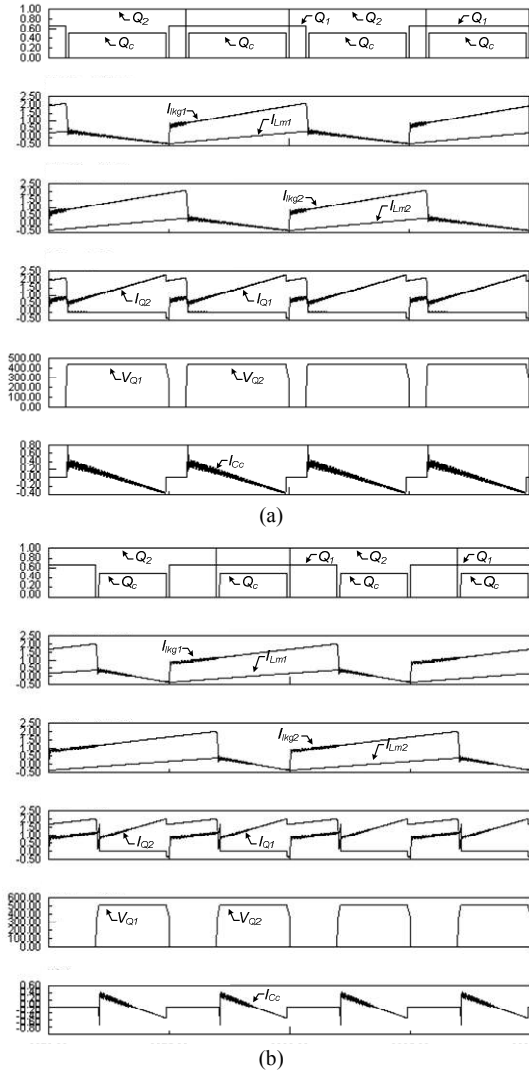


Fig. 5 Key simulation waveforms of  $D>0.5$  operation. (a)  $V_S=385\text{-Vdc}$ . (b)  $V_S=320\text{-Vdc}$ .

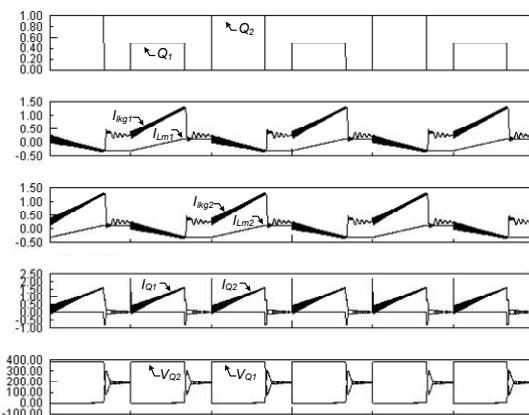


Fig. 6 Key simulation waveforms of  $D<0.5$  operation.

evaluation of interleaving technique in forward converters," *IEEE Trans. Power Electronics*, vol. 13, no. 4, pp.690-698, Jul., 1998.