Single-Phase Z-Source Matrix Converter (SZMC) with Output Voltage Boost Capability

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Abstract

This paper deals with a new single-phase Z-source matrix converter (SZMC) topology. Unlike other conventional configurations, the proposed SZMC is not only a step-up frequency converter but also a step-down frequency converter and a voltage boost capability. Thus, the proposed SZMC is also called a frequency step-up/down and voltage step-up converter. A safe-commutation strategy is used in SZMC as free-wheeling operation to eliminate voltage spikes on switches. The operating principles and experimental results of the proposed SZMC are presented.

1. Introduction

The ac output voltage cannot exceed the ac input voltage in the conventional SPMC(Single-Phase Matrix Converter) [1,2]. In addition, both bi-directional switches of any phase leg can never be turned on at the same time; otherwise current spikes generated this way will destroy the switches [3]. For applications where only voltage regulation is need, a family of single-phase Z-source ac-ac converters proposed in [4, 5] has merits such as providing a larger range of output voltage with buck-boost mode, reducing in-rush and harmonic current. When the ac-ac power conversion requires both variable output voltage and variable frequency, the converter based on Z-source structure and matrix converter topology have to realize.

In this work, the Z-source concept employs to SPMC to create a new converter called single-phase Z-source matrix converter (SZMC). Compared to the existing PWM ac-ac converters, the proposed SZMC can provide a wide range of output ac voltage operation in boost mode and step-up/down frequency. The operating principle and experimental results are shown that the proposed SZMC can boost voltage in frequency step-up/down operation with high efficiency. A safe-commutation strategy is also implemented as free-wheeling operation to eliminate voltage spikes on switches.

2. The principles

Fig. 1 shows the proposed SZMC. It employs a Z-source network, bi-directional switches and *R-L* load. All the inductors and capacitors are small and used to filter switching ripples. The symmetrical Z-source network, a combination of two inductors and two capacitors, is the energy storage/filtering element for the SZMC. Since the switching frequency is much higher than the ac source (or line) frequency, the inductor and capacitor requirement should be low [5]. As shown in Fig. 1, the proposed SZMC requires four bi-directional switches S_{1j}, S_{2j}, S_{3j}, S_{4j} ($j = a, b$) as SPMC and one source bi-directional switches S_{sj} ($j = a, b$), where 'a' and 'b' are representing drivers one and two, respectively. All bi-directional switches are common emitter back to back switch cells.

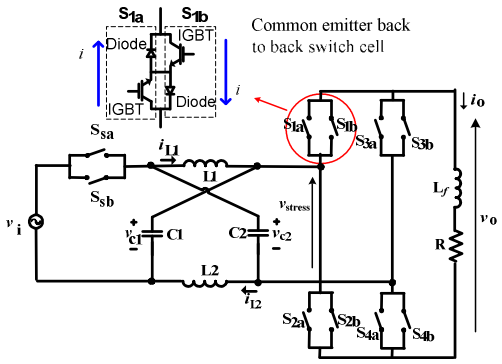

Fig. 1 Proposed SZMC topology

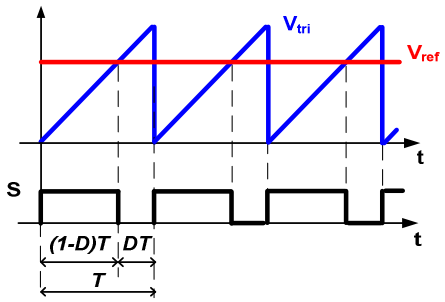

Fig. 2 Duty ratio control of switches

The proposed SZMC can be operated with PWM duty ratio control in exactly the same way as the conventional ac-ac converter. Fig. 2 shows the PWM control scheme for SZMC. As shown in Fig. 2, D is an equivalent duty-ratio; T is a switching period. Implementation of SZMC requires different bidirectional switching arrangements depending on the desired amplitude and frequency of output voltage. The amplitude of output voltage is controlled by the duty-ratio, D, while the frequency of output voltage depends on the switching strategy. In this work, the frequency of input voltage, f_i, is set at 60 Hz and desired output frequency, f_o, synthesized at the 120 Hz (step-up frequency), 60 Hz

(same frequency) and 30Hz (step-down frequency). As an example, the operation at 120 Hz output frequency of the proposed SZMC is released. Fig. 3 illustrates the switching strategy for one cycle of input voltage at 120 Hz output frequency. The operation of proposed SZMC can be divided into four stages as shown in Figs. 4 to 7.

Stage 1: (Both input voltage and output voltage are positive). The switches S_{sa}, S_{1a}, S_{2a}, and S_{4b} are fully turned on (S_{2a} turns on for commutation purpose; S_{sa} and S_{4b} turn on for continuous current flow purpose); S_{3b} and S_{4a} are modulated in complement with dead time. In state 1, as shown in Fig. 4(a), S_{4a} turns on and conducts current flow during increasing positive cycle of input voltage; S_{2a} turns on for commutation purpose. Then S_{4a} turns off and S_{3b} has not turned on, there are two occurring commutation states. If $i_{L1} + i_{L2} + i_{Lf} > 0$, the current path flows from S_{sa}, as shown in Fig. 4(b); if $i_{L1} + i_{L2} + i_{Lf} < 0$, the current path flows from S_{4a} and S_{4a}, as shown in Fig. 4(c). In state 2, as shown in Fig. 4(d), S_{3b} turns on and conducts current flow in Z-source network as shoot-through path; the load current may be freewheeled through S_{2a}, S_{1a}. In these switching patterns, the current path is always continuous whatever the current direction. Thus, the voltage spikes are eliminated during switching and commutation processes.

Stage 2: (The input voltage is positive; the output voltage is negative). The switches S_{sa}, S_{1b}, S_{2b}, and S_{3a} are fully turned on (S_{1b} turns on for commutation purpose; S_{sa} and S_{3a} turn on for continuous current flow purpose); S_{3b} and S_{4a} are modulated in complement with dead time. In state 1, as shown in Fig. 5(a), S_{3b} turns on and conducts current flow during decreasing positive cycle of input voltage; S_{1b} turns on for commutation purpose. In state 2, as shown in Fig. 5(b), S_{4a} turns on and conducts current flow in Z-source network as shoot-through path; the load current may be freewheeled through S_{1b}, S_{2b}.

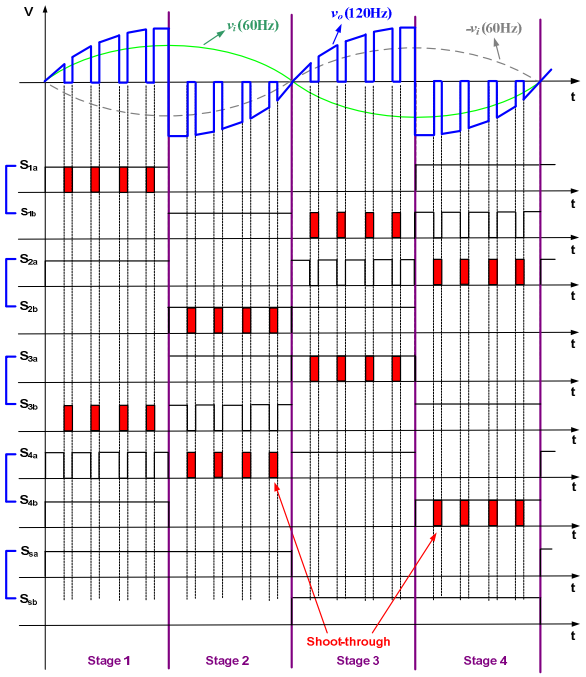

Fig. 3 Switching pattern of the proposed SZMC at 120 Hz frequency.

Stage 3: (The input voltage is negative; the output voltage is positive). The switches S_{sb}, S_{2b}, S_{3a}, and S_{4a} are fully turned on (S_{4a} turns on for commutation purpose; S_{sb} and S_{2b} turn on for continuous current flow purpose); S_{1b} and S_{2a} are modulated in complement with dead time. In state 1, as shown in Fig. 6(a), S_{2a} turns on and conducts current flow during increasing negative cycle of input voltage; S_{4a} turns on for commutation purpose. In state 2, as shown in Fig. 6(b), S_{1b} turns on and conducts current flow in Z-source network as shoot-through path; the load current may be freewheeled through S_{4a}, S_{3a}.

Stage 4: (Both input voltage and output voltage are negative). The switches S_{sb}, S_{1a}, S_{3b}, and S_{4b} are fully turned on (S_{3b} turns on for commutation purpose; S_{sb} and S_{1a} turn on for continuous current flow purpose); S_{1b} and S_{2a} are modulated in complement with dead time. In state 1, as shown in Fig. 7(a), S_{1b} turns on and conducts current flow during decreasing negative cycle of input voltage; S_{3b} turns on for commutation purpose. In state 2, as shown in Fig. 7(b), S_{2a} turns on and conducts current flow in Z-source network as shoot-through path; the load current may be freewheeled through S_{3b}, S_{4b}. The analysis of commutation states in stages 2, 3 and 4 is similar to that in stage 1. The dotted line in Figs. 4 – 7 indicates the safe-commutation switch during each particular stage.

The commutation switches need a period of overlap, t_o, between stages as shown in Fig. 8. The t_o is calculated to guarantee the load current goes to zero and Z-source network capacitor discharges before a new stage starts. In this work, t_o was found to be approximately 110 μs. Other operations at 60 Hz and 30 Hz output frequency are implemented by omitting stage 2, stage 3 and exchanging between stage 2 and stage 3, respectively.

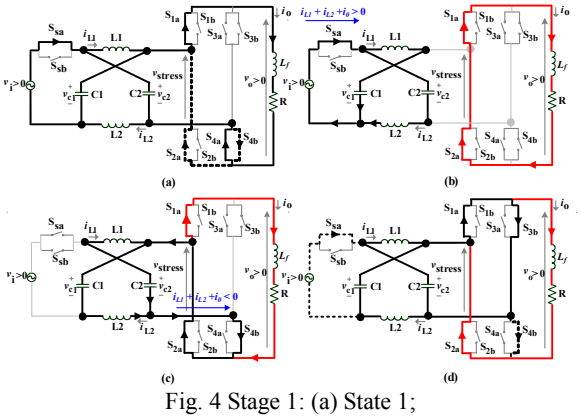

Fig. 4 Stage 1: (a) State 1;
(b) Commutation state when $i_{L1} + i_{L2} + i_{Lf} > 0$;
(c) Commutation state when $i_{L1} + i_{L2} + i_{Lf} < 0$; (d) State 2

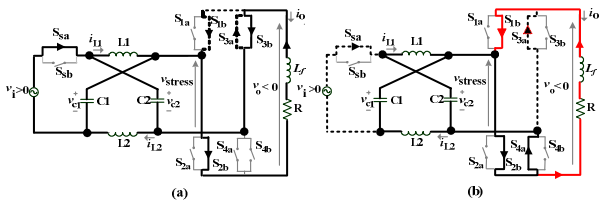

Fig. 5 Stage 2: (a) State 1; (b) State 2.

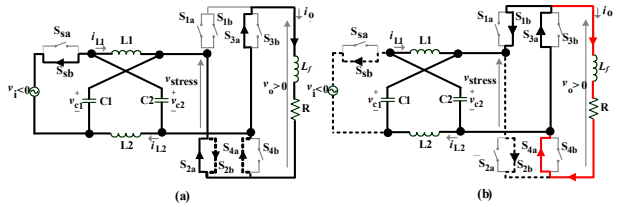

Fig. 6 Stage 3: (a) State 1; (b) State 2.

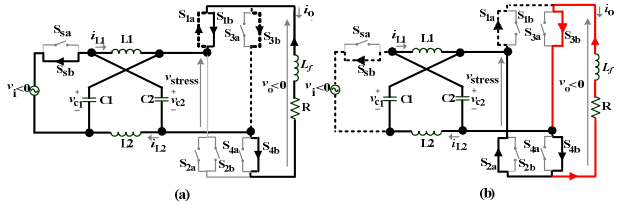

Fig. 7 Stage 4: (a) State 1; (b) State 2.

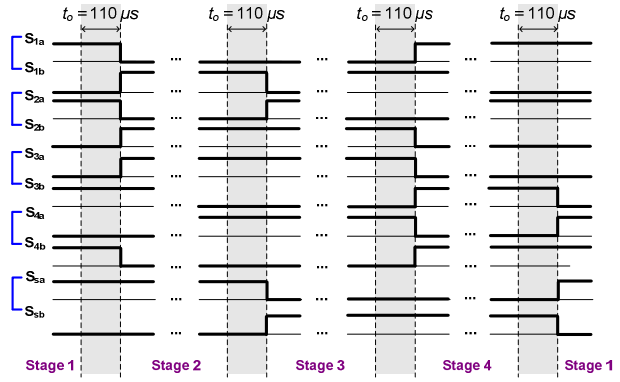

Fig. 8 Timing diagram for commutation strategy

3. Experimental Results and Discussions

To verify the analysis above, experiments have been performed and its parameters used are listed in table 1. Experiment is implemented for the proposed SZMC at V_i = 40Vrms (56Vpeak)/60Hz. Fig. 9, 10 and 11 show the experimental results at frequency of 120 Hz, 60 Hz and 30 Hz with D = 0.3, respectively. As shown in Figs. 9 - 11, when D = 0.3, the output voltage is boosted to about V_o = 60 Vrms from 40 Vrms input voltage. The voltage gain is approximate 1.5. Fig. 12 shows the relationship been output voltage gain (K) and duty cycle (D). By experimental results, we can observe that the output voltage can be boosted with variable frequency. It is clear that, as expected, the proposed SZMC is a frequency step-up/down and amplitude voltage step-up converter.

Table 1 Experimental parameters

Z-source network	L_1=L_2	1 mH
	C_1=C_2	1 μF
Switching frequency (f_{sw})		20 kHz
Dead time		0.5 μs
Overlap time (t_o)		110 μs
Duty cycle (D)		0.3
	R	100 Ω
	L	3 mH

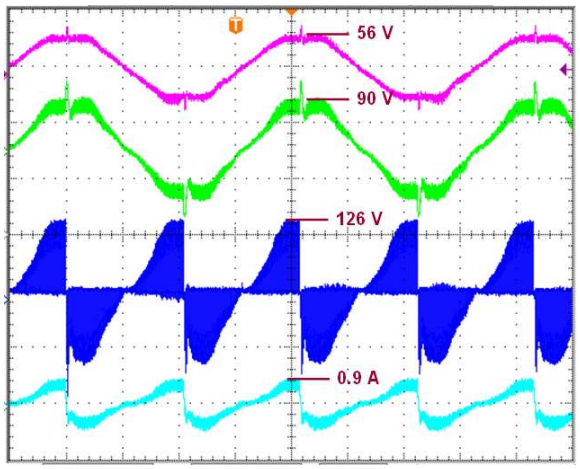

Fig. 9 Experimental result at frequency of 120 Hz with D = 0.3. From top to bottom: v_i (100V/div.), v_{C1} (100V/div.), v_o (100V/div.), i_o (2A/div.); t (4ms/div.).

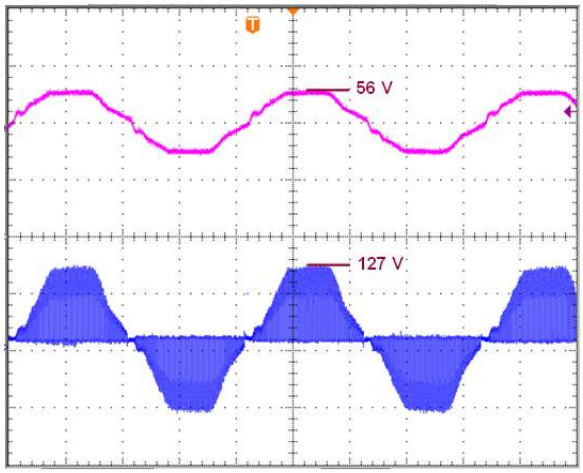

Fig. 10 Experimental result at frequency of 60 Hz with D = 0.3. (top: input voltage 60Hz; bottom: output voltage 60Hz) (x-axis: 4ms/div; y-axis: 100V/div)

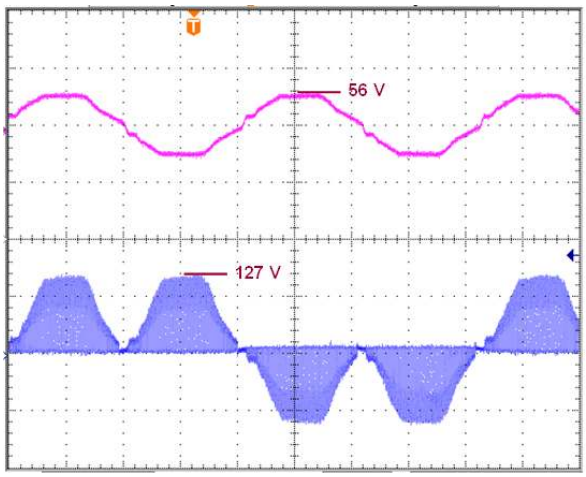

Fig. 11 Experimental result at frequency of 30 Hz with D = 0.3. (top: input voltage 60Hz; bottom: output voltage 30Hz) (x-axis: 4ms/div; y-axis: 100V/div)

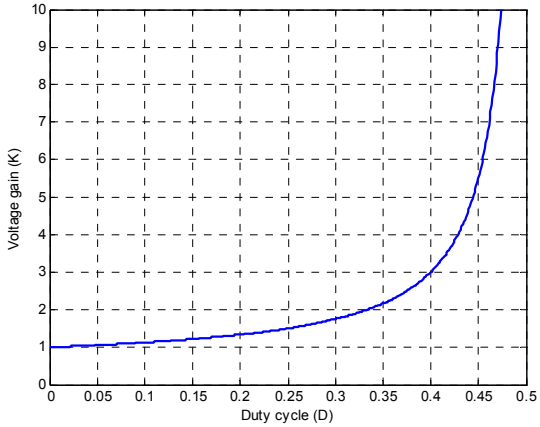

Fig. 12 Relationship between output voltage gain (*K*) and duty cycle (*D*).

4. Conclusions

This paper has proposed a new single-phase Z-source matrix converter (SZMC) with output voltage boost capability. The proposed SZMC can boost to a desired output voltage with variable frequency. Thus, the proposed SZMC is a frequency step-up/down and amplitude voltage step-up converter. In order to provide a continuous current path, the commutation strategy is employed. Steady-state analysis, operation stages, experimental results were presented. Further research is also carried out with wide range operation regions in buck-boost voltage mode. Thus, the proposed SZMC can be also called an amplitude voltage step-up/down and frequency step-up/down converter. For applications where both variable output voltage and variable frequency are need, the proposed SZMC is a better choice to achieve high efficiency, low harmonic current in line, smaller size and lower cost.

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