FPGA Based PWM Generator for Three-phase Multilevel Inverter

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Abstract

This paper deals with the implementation on a Field Programmable Gate Array (FPGA) of PWM switching patterns for a voltage multilevel inverter. The reference data in main microcontroller is transmitted to the FPGA through 16 general purpose I/O ports. Herein, three-phase reference voltage signals are addressed by the last 2-bit (bit 15-14) and their data are assigned in remaining 14-bit, respectively. The carrier signals are created by 16-bit counter in up-down counting mode inside FPGA according to desirable topology. Each reference signal is compared with all carrier signals to generate corresponding PWM switching patterns for control of the multilevel inverter. Useful advantages of this scheme are easy implementation, simple software control and flexibility in adaptation to produce many PWM signals. Some simulations and experiments are carried out to validate the proposed method.

I. INTRODUCTION

In recent years, many applications in industry have demanded higher power equipments. A single power semiconductor switch may be requested to directly connect to medium voltage grids, even up to 6.9 kV, for operation of a controlled ac drives in the megawatt range. Today, the rating parameter of a power semiconductor switch does not suit for those requirements. In addition, in power conversion, a small voltage steps can yield waveforms with low harmonic distortion as well as small dv/dt. For these reasons, a new family of multilevel inverters has become increasingly popular due to its advantages. It has emerged as the solution for working with higher voltage levels and producing low harmonic distortion in the output waveforms. [1]

Multilevel inverters are combined from a lot of power semiconductors and capacitors in many topologies which are outstanding as diode-clamp multilevel inverter, capacitor-clamp multilevel inverter, H-bridge cascade multilevel inverter and so on.[2] Its output voltages are with stepped waveforms with low harmonic component. By using above mentioned topologies, the power semiconductor in multilevel inverter can only withstand a stress voltage which is lower than its rating. Along with its advantages, the multilevel inverters also require a complex control algorithm and tough hardware design. A lot of PWM signals must be generated for controlling many power switching devices of the multilevel inverter that can be over the capacity of a current microcontroller. For overcoming this obstacle, a FPGA is utilized to generate the switching patterns for a multilevel inverter. Many studies on the multiform scheme for producing PWM control signals based on a FPGA are proposed so far, but almost those schemes are complex and tough in implementation. [3], [4]

In this paper, an implementation on a FPGA based PWM generator for a voltage multilevel inverter is presented. Herein, the reference data in main microcontroller is transmitted to the FPGA through 16 general purpose I/O ports. Three-phase reference voltage signals are addressed by the last two bits (bit 15-14) and their data are assigned in remaining fourteen bits, respectively. The carrier signals are manufactured by 16-bit counter in up-down counting mode inside FPGA. The M-based carrier signal and W-based carrier signal are created according to desirable topology. The remaining carrier signals can be obtained by level-shift these based signals by an offset factor which is determined from the inverter level and the peak value of reference control signal. After decoding, each reference signal is compared with all carrier signals to generate corresponding PWM switching patterns for control of the multilevel inverter. This method has some advantages in implementation, simple software control and flexibility in adaptation to produce many PWM signals. Some simulations and experiments are fulfilled to validate the proposed method.

II. PRINCIBLE OF OPERATION

Block diagram of the proposed scheme is shown in Fig1. Inside main microcontroller, the reference data obtained from motor drives algorithm is transferred to the FPGA through 16 general purpose I/O ports. Three-phase reference voltage signals are addressed by the last two bits (bit 15-14). Two-bit address can be figured out such as *00* for V_{sa}, *01* for V_{sb} and *10* for V_{sa}. The instant value of each reference signal is assigned in remaining fourteen bits, respectively. The FPGA based PWM generator manufactures the desirable PWM switching

pattern, which is suitable to the given strategy, to control the multilevel inverter.

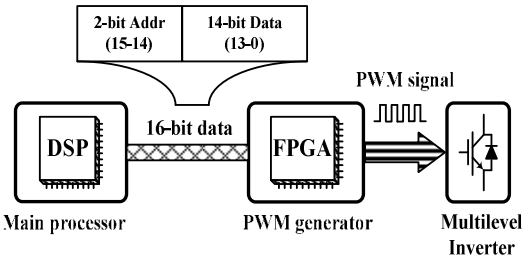

Fig.1 Block diagram of the proposed scheme

The closed view of the proposed PWM generator is depicted in Fig. 2. Herein, the carrier signals are established by 16-bit counter in up-down counting mode inside FPGA. The M-based carrier signal or the W-based carrier signal or even both of those based signals are created according to desirable topology. The remaining carrier signals can be obtained by level-shift these based signals by an offset factor, *K*, which is determined from the inverter level and desirable data resolution.

For instant, the number of inverter level is *m* and the reference data is described in *n-bit* data, then the offset factor can be calculated as follows

$$K = \frac{2^n}{m-1} \qquad (1)$$

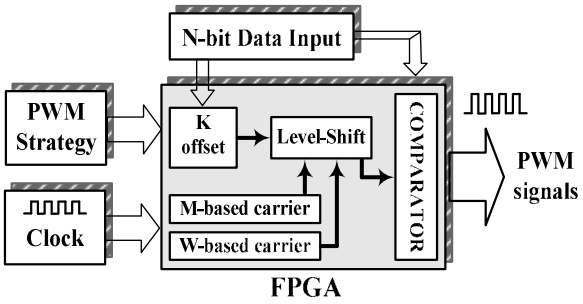

Fig. 2 The proposed PWM generator

Fig. 3 briefly illustrates the reference and carrier signals in the typical phase disposition (MMMM) method. For the case of *m-level* inverter, (*m-1*) carrier signals are required for controlling all switching devices in the inverter module. In this case, the M-based carrier signal is produced firstly and then the next carrier signal can be archived by shift a value of K from the previous one.

All carrier signals after level-shifting are compared with n-bit reference data to create the expected PWM switching pattern.

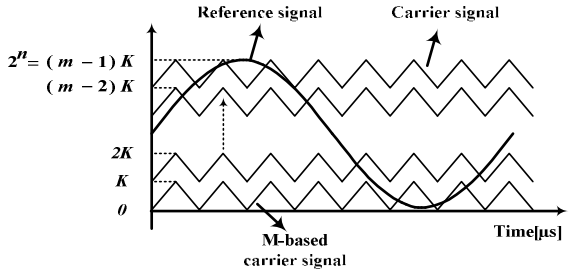

Fig. 3 Typical strategy PWM based carrier

III. IMPLEMENTATION AND RESULTS

The development of field programmable gate array ICs during the last years provides an alternative solution for the implementation of digital power converter control units. They have the advantage of flexibility due to their reprogramming capability, while their operating frequency can be as much as hundreds of MHz. FPGAs have been used in power electronics applications for the implementation of complicated control schemes.

In order to verify the proposed scheme, a PWM generator for a nine-level diode-clamp multilevel inverter is built. An Altera-FLEX family FPGA (EPF10K40RC208-3) is selected for the given implementation. The inverter is designed to operate at *5KHz* frequency. A DSP 32-bit TMS320F2812 is uses as main microcontroller to control and transfer *14-bit* reference data to the FPGA. Obviously, the offset factor, *K*, can be obtained as a value of *2048* according to (1). It strongly recommends utilizing a *10.24MHz* oscillator as clock source for FPGA to get exactly *200μs* sampling period.

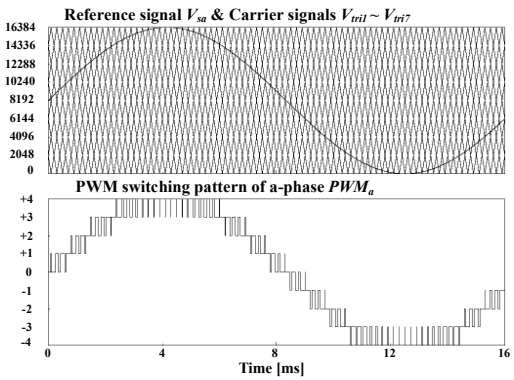

Fig. 4. Simulation of the PWM switching pattern

The output PWM switching pattern, which is created by the proposed scheme, for a-phase of a nine-level inverter can be drawn in Fig. 4. In this simulation, MWMW scheme is utilized to get a low harmonic distortion output voltage. the phase-a reference signal V_{sa} and eight carrier signals are shown in top trace, whereas the nine-level switching pattern is visualize in bottom one.

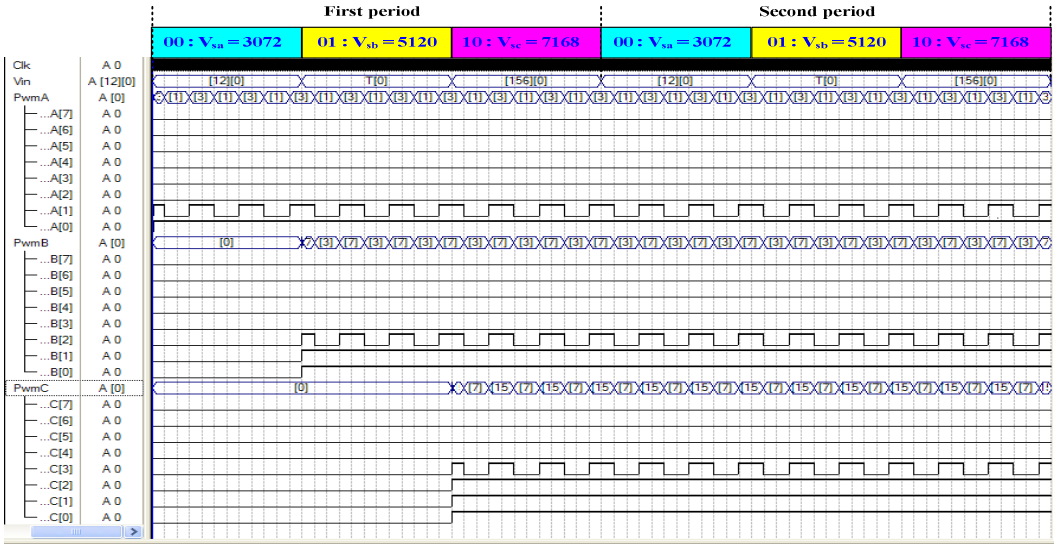

Fig. 5. Output PWM signals by simulation with Quartus II

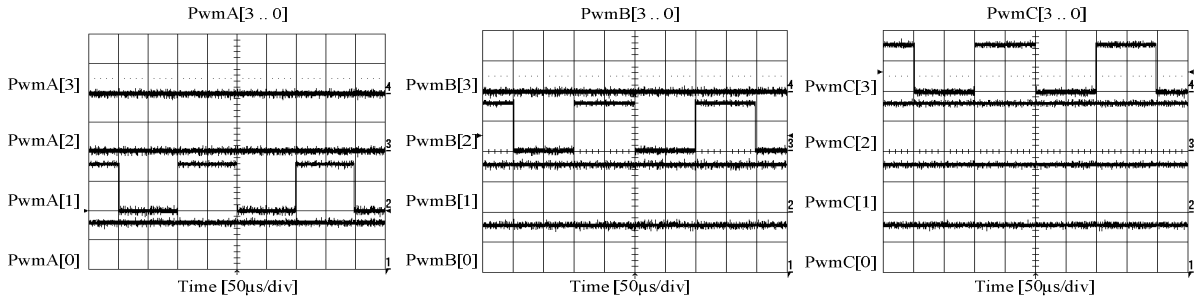

Fig. 6. Output PWM signals by experiment with an Altera FPGA

Fig. 5 illustrates the simulation result with the proposed algorithm using QuatusII software. Three-phase reference data are assigned as fixed value such as V_{sa} = *3027*, V_{sb} = *5120* and V_{sc} = *7168* to generate *50%* duty cycle at *PwmA[1]*, *PwmB[2]* and *PwmC[3]*, respectively. Obviously, V_{sa} intersects the carrier signal number two at its middle point, so the output *PwmA[1]* has 50% duty cycle as expectation. The *PwmA[0]* is always high state because its carrier signal locates lower than the corresponding reference. All remaining output PWM signals of phase-a are low state in this case. The other phases behave in the similar way. Up to now, it can conclude that the simulation result quite satisfy the given requirement. Fig. 6 shows the experimental result at the same condition with that of simulation. It is clearly that the result verifies very well the simulation as well as the proposed method.

IV. CONCLUSION

The implementation of PWM generator based on a FPGA for the voltage multilevel inverter is presented in this literature. The advantages of this scheme are easy implementation, simple software control and flexibility in adaptation to produce many PWM signals. Some simulation studies by QuartusII software and experiments by a DSP 32-bit TMS320F2812 and an Altera FPGA are carried out to verify the suggested method.

ACKNOWLEDGMENT

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