0.18 ㎛ CMOS Quadrature VCO for IEEE 802.11a WLAN Application

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Abstract

The proposed CMOS Quadrature VCO for WLAN application was designed in TSMC 0.18 ㎛ RF CMOS technology. The QVCO based on NMOS back-gate as a coupling transistor and switched capacitors array without tail transistors is designed to generate quadrature output signals. The simulated results show that the QVCO core consumed 3.67 ㎃ and 6.6 ㎽ from a 1.8 V supply. The QVCO is tunable between 4.76 ㎓ ~ 6.35 ㎓ and has a phase noise lower than -116.8 dBc/㎐ at 1 ㎒ offset over the entire tuning range

I. Introduction

In recent years, considerable amount of the wireless industry's effort has been focused on high level integration of the radio systems in CMOS technologies for cost reduction, especially in the 802.11a WLAN areas. The frequency band of IEEE 802.11a has the lower band 5.15~5.35 ㎓ and upper band 5.725~5.825 ㎓. In order to meet the requirements of the IEEE 802.11a standard, the QVCO should also cover the frequency range of 5.15 ~ 5.825 ㎓ and has a phase noise performance of at least -110 dBc/㎐ at 1 ㎒ offset from carrier.

To implement an 802.11a WLAN receiver, a direct conversion receiver (DCR) is more suitable for the integrated-circuit design than a heterodyne receiver, since an external image reject filter is not required.[1]

Many direct conversion architectures require in-phase and quadrature-phase signals from a local oscillator. The I and Q signals can be obtained by the combination of a direct connection and a cross connection force the two VCOs to oscillate in quadrature. [2]

II. Design of QVCO

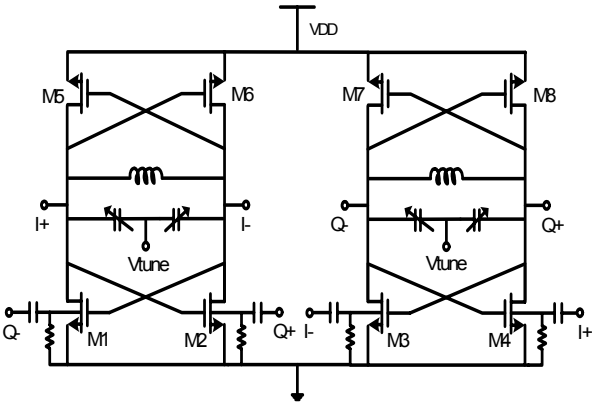

Fig 1. QVCO schematic

Figure 1 shows the implemented QVCO schematic. The QVCO consists of two complementary cross-coupled differential LC oscillator and the two oscillators are coupled directly by the NMOS back gate for the quadrature outputs.

If we use complementary cross-coupled differential LC oscillator, less current consumption is possible due to the additional pMOS transistors used for negative conduction generation. besides better waveform symmetry can be achieved through proper sizing of the transistors. As results, phase noise reduced.

The NMOS back-gates to couple the signals between the two differential VCO, instead of the transistor used to implement QVCO. Because this topology is not required additional coupling transistors, We can reduce the power consumption and good phase noise. The resistors are adopted for DC biasing of the body terminals and the

capacitors for AC coupling. [3] Furthermore the current source was omitted to maximize the signal swing and get better phase noise performance.

The LC tank consists of MOS varactors, symmetry inductors, 3bit switched capacitors array induce the required oscillation frequency. One of the main goals of this design is to concurrently achieve low phase noise and a wide frequency tuning range. Single varactor device with steep C-V characteristic can be used to achieve a wide frequency range. However, this can result in an excessively high tuning sensitivity Kvco. To avoid this problem, by using a 3bit switched capacitor array, a wide tuning range can be achieved stably against the process variation.

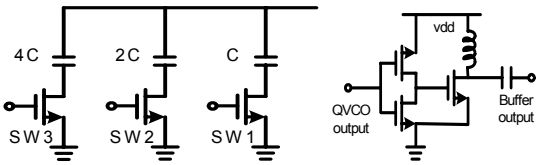

Fig 2. 3bit Switched capacitor array and output buffer schematic

These 3bit switched capacitor array can change the parasitic capacitances of LC tanks, and thus affect the oscillation frequency where the 3bit switched capacitors are implemented by using MIM capacitors. NMOS devices are used to switch each capacitor in and out of the tank. [4] While a control voltage is tuned from 0 to 1.8 V. The maximum tuning sensitivity can reach to 220 ㎒/V.

MOS varactor applied minimum value which has high quality factor and symmetry inductor of 2.54nH with Q-factor of 12.2 at 5.5 ㎓ is used.

Ⅲ. Simulation Result

The designed QVCO is implemented using TSMC 0.18㎛ CMOS process. The simulated results show that the QVCO core consumed 3.67㎃ and 6.6㎽ from a 1.8V supply (total QVCO consumed 7.5 ㎃ and 13.5 ㎽) Fig 3. shows Frequency tuning curve, The QVCO is tunable between 4.76 to 6.35 ㎓, and It reaches the tuning range of 25%.

Fig 4. shows simulated time-domain outputs and Phase noise performance. The worst noise is -116.8 dBc/㎐ at 1㎒ offset over the entire tuning range. All of these performances satisfy the IEEE 802.11a standard.

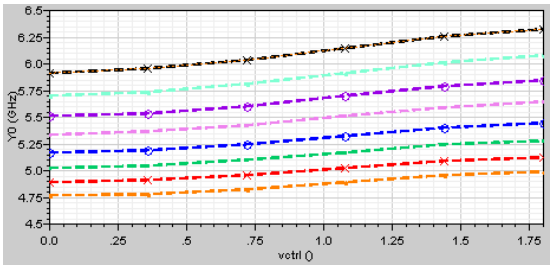

Fig 3. Frequency tuning curve

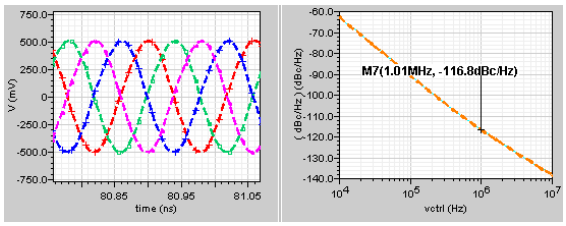

Fig 4. Simulated time-domain outputs and Phase noise performance

Ⅳ. Conclusion

In this paper, proposed QVCO based on NMOS back-gate as a coupling transistor and switched capacitors array without tail transistors is designed to generate quadrature output signals.

This simulation meets the specification for 5.25 ㎓ band (5.15~5.35 ㎓) and 5.8 ㎓ band (5.725~5.825 ㎓) of the IEEE 802.11a WLAN standard.

Acknowledgement

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Reference

[1] Liang-Hui Li et al, "Complete RF-System Analysis of Direct Conversion Receiver for 802.11a WLAN OFDM System" IEEE Trans. On Vehicular Tech, Vol 56, no. 4 pp. 1696 - 1703, JULY. 2007.

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