Two-bit/cell SONOS flash memory device utilizing a modified saddle structure

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I. Introduction

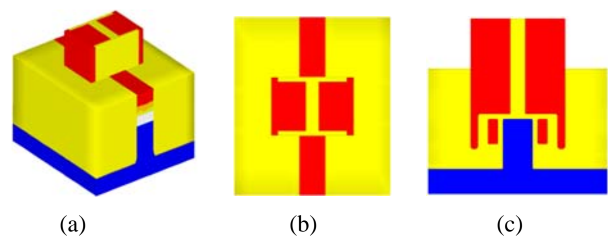
As the needs of high-density memory are explosively increasing, multi-bit operation has received great attentions [1]. There are two typical approaches to obtain two-bit memory. One is multi-level operation using large V_{TH} window, commonly used in floating gate-type cells and the other is twin-bit operation using localized charge trapping, commonly used in SONOS-type cells[2].

The saddle structures remarkably enlarge effective channel width and suppress short channel effect (SCE). In this study, we have realized a novel structure by combining SONOS as a multi-bit with the saddle structure to obtain both the easy off-leakage controllability and the superior current drivability[3-5]. The Modified Saddle SONOS structure is expected to be very useful for the high-speed and low-power consumption devices. The major transistor characteristics of modified saddle SONOS device are investigated and discussed through the comparison with the SONOS and the saddle MOSFET, including their threshold voltage (Vth)dependencies.

This paper reports a new cell concept for two-bit/cell SONOS memory by adopting recessed channel region covered with nitride layer for the charge storage. We consider comparison with conventional planar channel SONOS memory device and the effect of channel doping profile and drain bias. Device processes and characteristics of the modified saddle SONOS flash memory cells were investigated by using TAURUS PROCESS and TAURUS DEVICE conventional simulators, and the simulated results of the proposed SONOS flash memory were compared with those of conventional SONOS flash memory. Therefore, studies concerning designs of increasing storage capacity density reading and programming speeds are necessary for enhancing the efficiencies of the multilevel NAND flash memories.

II. A Proposed Modified Saddle SONOS Flash Memory Structure

Figure 1(a) and 1(b) shows the cross-sectional views across the gate and the thin body and top view of the modified saddle SONOS flash memory cell. Figure 1(c) show the three-dimensional views of the modified saddle SONOS flash memory cell.



(a) (b) (c)

Figure 1. (a) Three-dimensional view, (b) top view, and (c) front view of proposed flash memory device.

Saddle and gate geometries are defined in the mask layer. The source/drain doping implant is done. Arsenic is implanted vertically with a dose of $4.0 \times 10^{15}cm^{-2}$,with an energy of 20KeV. After the vertically stacked layer consisting of the tunneling oxide layer, the floating gate poly-Si layer, the blocking oxide layer, and the control gate poly-Si layer are sequentially formed on the etched and boron-doped Si substrates with a low doping concentration of $1\times10^{18}cm^{-3}$. The physical control gate width is 30nm. The thicknesses of the tunneling oxide, the poly-Si, and the blocking oxide of ONO layers are 4, 4, and 6 nm , respectively.

III. Simulation Results

Figure 2 is the result to simulate trap charge densities as change program bias for the nitride of the SCG NAND CTF memory cell of the initial stage. Figure 2 and 3 show current-voltage (I-V) characteristics of after programming and erasing by FN-tunneling electrons to the storage node of modified saddle SONOS device with a gate length of 40 nm. Figure 4 shows drain currents as functions of the Control Gate voltage (I_D-V_{CG}) at an initial stage before performing the program operation. Program bias condition is CG1:0V, CG2:12V. I_D-V_{CG2} characteristic curves show that the value soft the threshold voltages and the driving currents are same.

Table I. The simulation parameters of the proposed memory cell.

Contents	Modified Saddle SONOS flash memory cells
Program voltage (V)	V_{WL}=10~12/V_{BL}=V_{SL}=V_{SUB}=0
Program time (ms)	1
Read voltage (V)	0~5
Erase voltage (V)	V_{WL}=-12/V_{BL}=1~4,V_{SL}=V_{SUB}=0
Erase time (ms)	1

IV. Summary and Conclusions

We have proposed two-bit/cell SONOS flash memory devices with nitride charge trapping layer in saddle structure for high density and high performance. It has good program/erase operation, good SCE immunity. A new flash concept has been introduced. It is based on charge trapping in a dielectric layer and on a saddle structure. This cell can store two bits, which are operated independently, thus reducing even further the area per bit. By controlling the channel doping profile in terms of peak concentration, we achieved successfully two-bit/cell operation.

Acknowledgements

This work was supported by the National Program for Tera-level Nano-devices of the Ministry of Science and Technology as one of the 21st century Frontier Programs.

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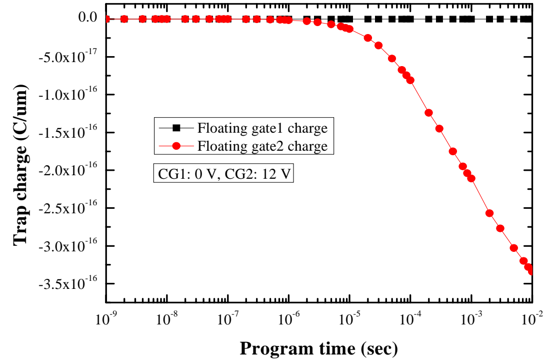

Figure 2. Trap charge densities as functions of the Program time for the modified saddle SONOS cell

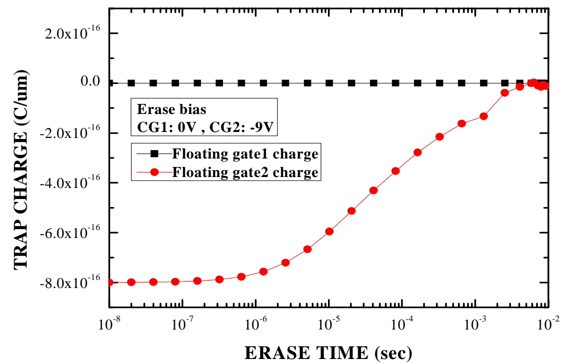

Figure 3. Trap charge densities as functions of the erase time for the modified saddle SONOS cell

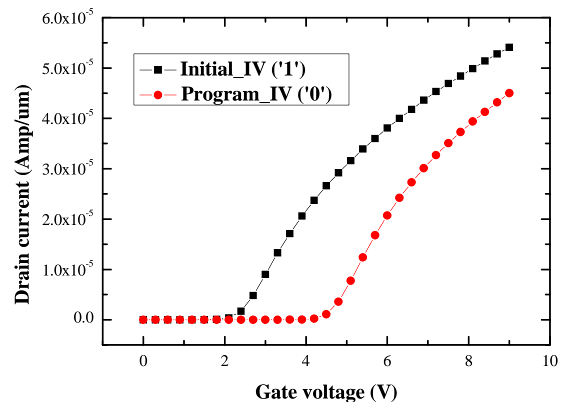

Figure 4. Drain current as functions of the Control Gate voltage (I_D-V_{CG})