The DFM-Aware Design with Statistically-based Approaches in 130nm and below

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Abstract

As technology continues to scale down dramatically into 130nm and below, the impacts of process-induced variations on interconnect as well as device become more severe and significant in 130nm and below design. In order to predict changes of circuit characteristics due to process-induced variations accurately and efficiently, the DFM-Aware design environment has been developed and verified.

I. Introduction

Designer has to consider it in their design, called Design-for-Manufacturing (DFM). Current concept of DFM is not really manufacturing-aware[1]. Also, the designer has to resolve DFM issues from a design flow point of view and not from a point-tool point of view because DFM issues have to be considered from design to manufacturing [2]. A new DFM-Aware design environment has been developed for modeling method for algorithm of non-normal distribution handling that were treated as normal distributions, and inconsistency among primitive interconnect structures.

II. DFM-Aware Design

The DFM-Aware design environment has been implemented on Sun Solaris O.S. 9 with standard C/C++, Tcl/Tk 8.4, and BLT 2.4. The main engine part and GUI part have been developed separately for the platform independent because GUI is strongly dependent on the platform. BLT toolkit is an extension version of Tcl/Tk. This toolkit has been used for a part that is difficult to implement with Tcl/Tk such as a busy widget and a background execution. As shown in Figure 1, it consists of two major parts: model generator and model applicator. The model generator has been developed to provide interconnect characterization and models/DB generation with statistical approaches. The model applicator has been developed to apply worstcase model to Front-End-Of-Line (FEOL) such as Place and Router, Schematic Capture, and Timing Analysis Tools.

To verify DFM-Aware design environment, accuracy and speed are verified. 31-stage ring oscillators which are designed and fabricated with 0.13mm logic process are measured. To confirm flexibility with other technology nodes, 15-stage ring oscillators which were designed and then fabricated with 0.18mm standard CMOS process is measured.

As a results, it improves the accuracy by more than two times and the CPU time by 29.61% ~ 32.01% when compared to that of conventional worstcase interconnect simulation for both 0.13mm and 0.18mm process [3]. The result confirms that the worstcase interconnect design environment with the new worstcase optimization algorithm predicts the worstcase interconnect models more accurately, rapidly, and efficiently. It accurately simulates not only normal distribution but also non-normal distribution which conventional methods cannot do well.

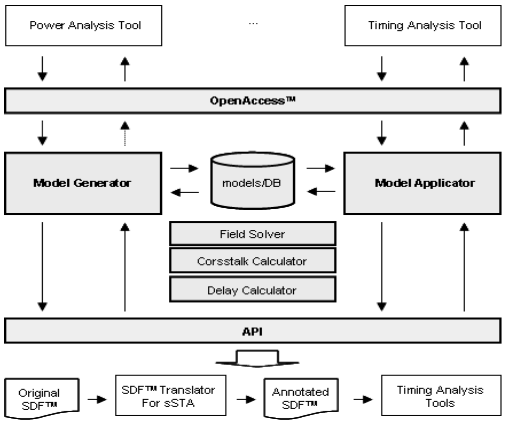

Figure 1. DFM-Aware Design Environment

The interface concept of the DFM-Aware design environment shown in Figure 2.

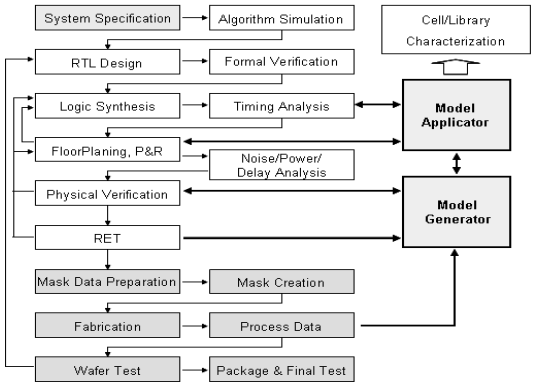

Figure 2. Integration of Standard Design Flow

The previous corner-based Static Timing Analysis (STA) which was used for circuit timing verification is not accurate in 90nm design and below. As a result, the statistical timing analysis is proposed as an alternative solution. It performs systematic modeling of the delay time caused from process-induced variations. Figure 3 shows application of statistically-based timing analysis with PrimeTime™ for digital circuit. It has been developed under the OpenAccess™ environment. The output of Verilog™ is imported into OpenAccess™ via OpenAccess™ interface. The SDF™, including the critical net information, goes to the API, and the API generates SPEF™. The PrimeTime™ calculates delay for the given critical net, and the result of PrimeTime™ goes directly into OpenAccess™.

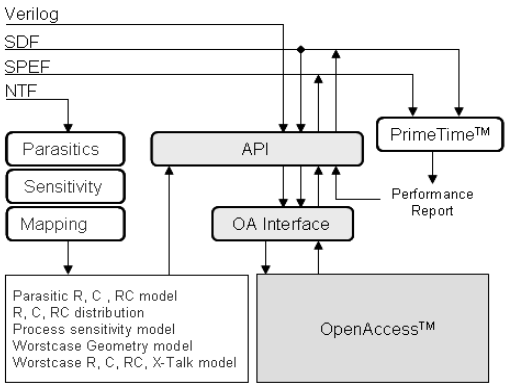

Figure 3. Application of Statistically-based Timing Analysis with PrimeTime™

Ⅲ. Conclusion

Consequently, new DFM-Aware design environment helps design with high accuracy and speed, and the interconnect effects due to process-induced variations can be applied to designs in 130nm and below. Eventually, the designer improves the performances of circuits and enhances the parametric yield of the circuit by considering design for-manufacturing and yield (DFM & Y) in 130nm and below design.

References

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[2] W.-Y. Jung, Journal of Electronic Design, August 2007.

[3] W. -Y. Jung, et al, IEICE TRANS. On Fundamentals of Electronics, Communications and Computer Sciences, pp.1177 -1184, Vol. E91-Q, No.4, April 2008