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Electrical properties of u/TaN/SiOC(-H)/p-Si(100) low-*k* dielectric stack

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Ongoing miniaturization is indispensable for enhancing the speed of ultra-large scale integration (ULSI) technology. However, reducing the distance between wiring increases the capacitance of that wiring, result in a signal propagation delay. To solve this problem, there is a need for novel interlayer dielectric materials with low dielectric constants ($k < 2.5$). Even in package level power isolation capacitors, improvements in performance are becoming more difficult and new materials are needed. Thechallenges to dielectric materials will become even more severe as the industry approaches the 10 nm generation. In this study, we report on the electrical properties of Cu/TaN/SiOCH/p-Si(100)/Al and Cu/TiN/SiOCH/p-Si(100)/Al, metal-insulator-semiconductor structures. Low dielectric constant SiOC(-H) thin films are deposited with different flow rate ratio by using plasma enhanced chemical vapor deposition (PECVD). The electrical properties of these MIS structures, such as interface states density, fixed oxide charge and leakage current density are calculated from the capacitance-voltage (C-V), conductance-voltage (G-V) and current-voltage (I-V) characteristics. Furthermore, the density distribution of interface states of the MIS structure is obtained from the forward bias of I-V characteristics. The experimental results will be presented and discussed in detail.