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Silicon Nanocrystal Non-volatile Floating Gate Memory Devices By Using Schottky Barrier Source/Drain (S/D) Structure

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Nowadays, conventional floating gate (FG) nonvolatile flash memories have been noticed encounting several scaling limits beyond 65nm generation. This scaling limit can be delayed by several steering technologies. To alleviate the scaling limitations of conventional FG device, One way will use Si nano-dots floating gate as charge storage. So the research of a novel memory device using Si nano-dots floating gate memory (NFGM) devices, has attracted very much attention. Also as the feature size of the device (the metal-oxide-semiconductor field-effect-transistor: MOSFET) has been scaled down to several deca-nanometer regime, the technologies face many challenged. For scaling down MOSFET, the formation of an ultra shallow source/drain(S/D) junction is essential. The ultra-shallow junctions and abrupt impurity profiles are required for doped S/D to immunize short channel effect. In these problems, the Schottky S/D MOSFET has the potential to be scaled down to the nanometer regime, because low electrode resistance with a very shallow extension can be realized using metal S/Ds. Moreover, the structure is quite simple and the ultra shallow junction can formed easily and accurately. So we had fabricated the nonvolatile floating gate memory device with Si-nanocrystal by using Schottky Barrier structure. Erbium is chosen as the source and drain metal of n-type Schottky barrier MOSFETs, because of its low schottky barrier height for electron.

The fabrication processes began with the <100> p-type silicon-on-insulator(SOI) wafer (14~24 Ωcm). A thin tunnel oxide (~5 nm) was grown by dry oxidation and then a layer of uniform Si-nanocrystal dots with a FWHM of 6±1nm and a density of $7x10^{11}$ cm^{-2} was deposited by a digital gas-feeding method in the LPCVD process.[1] And the control oxide was deposited 30 nm thick SiO2 using LPCVD at 400 ℃, and the gate electrode was deposited highly phosphorus doped n-type polycrystalline silicon. Ploy gates are patterned and then sidewall spacer is formed by using thermal oxidation method (sample 1) and by using low temperature oxide (LTO) deposited at 400 ℃ (sample 2). After blanket dry etching

of gate sidewall spacer, Erbium silicide in the source/drain was grown by RTA process after Erbium was sputtered and non-reacted erbium removed by wet etch in Sulphuric-acid hydrogen Peroxide Mixed (SPM) solution.

We achieved the memory window of NC is 4V. Program/erase time was 10ms/10ms for 18V/-18V respectively. The endurance property in terms of the initial memory window was maintained until 10,000 cycles.

[1] Chan Park, Kyoungmin Kim, Eunkyeom Kim, Junghyun Sok, Kyoungwan Park, Moonsup Han, Materials science and engineering B, Volume 140, Issues 1-2, 25 May 2007, Pages 103-108