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Proposed Driving Waveform for Improving Address Discharge Characteristics of AC PDP

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A new reset driving waveform is proposed to improve an address discharge time lag in this research under the conventional address voltages. The new reset waveform can accumulate the more wall charges between address-scan (A-Y) electrodes than those for conventional waveform. In this experiment, it is found that the formative time lag and statistical time lags could be reduced by the new reset waveform. The formative time lag with the new reset waveform was decreased by an amount of 200 ns and 100 ns, when the applied address voltages are varied from 60 to 100 V. It is also noted that the statistical time lags were decreased by an amount of 500 ns and 100 ns for these address voltage ranges.

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