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# Integration of Carbon Nanotubes for the Electronic Device Applications

**Wanjun Park**

Department of Electronis and Computer Engineering, Hanyang University
wanjun@hanyang.ac.kr

Sincethe discovery of carbon nanotubes (CNTs), extensive studies on this newcarbon allotrope have formed a new epoch in various fields of science and technology with their excellent physical and electrical properties, and chemical functionality. In particular, understanding of their electrical properties has aroused many researchgroups in academy and industry to explorethe nano-scale electronics based on CNTs such as transistor, memory, interconnect, logic array, and so on.Although the CNT-based electronics is regarded as a strong potential candidate for the next generation electronic devices, many technological barriers are still remained.

Pure nanotubes should be separated from a mixture of single-walled, multi-walled nanotubes, and carbonaceous impurities or should be grown without impurities for reliable device performance. Uncertainty and uncontrollability in positioning nanotubes on a right region is also a critical barrier for device integration. In addition, transport mechanism should be more understood to modulate band gap of them to fabricate various device elements.

In this presentation, we discuss our recent efforts to overcome the barriers focusing on transistors based on single-walled carbon nanotubes (SWNTs). Experimental and theoretical studies to control the CNT electronic structure are discussed for CNT-field effect transistors. The large scale fabrication of CNT electronic elements are also given for the selective growth of CNT that is extendable to device integration. Our transistor scheme uses directly grown SWNTs by water-plasma chemical vapor deposition. The technique includes low temperature growth below the glass deformation, avoidance of the metallic paths to solve density control problem, and application of transparent substrate and gate materials. Moreover position selective growing gives an advantage for transistor fabrication by leaving out the etching process for SWNTs. In fact, this technique allows us to statistics of on-off ratio from the transistor arrays. For the positioning problems, direct photolithographic method using a mixture of catalytic precursors and conventional resists as a catalytic resist is introduced with other positioning methods of nanotubes.