Compact Wilkinon Power Divider Design and Simulation Using IPD Technology

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Abstract : The wireless communication revolution has spawned a revival of interest in the design and optimization of radio transceivers. Radio transmit modules continue to shrink in die size and cost, requiring novel approaches for integration of the numerous passive elements of the radio front-end. A 3 dB Wilkinson power divider based on GaAs substrates, for DCS 1710-1880 MHz band was designed and fabricated showing excellent performance.

Key Words : Integrated Passive Devices, Wilkinson Power Divider, GaAs substrate, DCS

1. Introduce

Integrated Passive Devices (IPDs) have attracted much attention in recent years, primarily due to the needs of handheld wireless devices to further decrease in cost and size and increase in performances [1, 2]. In mobile phone communication system, the usage of IPDs is much smaller, precise, repeatable, have less tolerance on component values, better mass production reliability, and also a cost down for SMT, comparing to traditional discrete passives as shown in Figure 1. Many function blocks, such as harmonic filters, couplers, baluns, and power combiners/dividers, in the RF modules can be realized by using IPD technology [3, 4, 5]. Figure 2 indicates several passive devices that would lend themselves to integration via an Integrated Passive Device (IPD) Technology. Due to the facts that IPDs are generally fabricated using standard wafer fabrication technologies such as thin film and photolithography processing, they can be manufactured with low cost and small size with excellent reproducibility. In this paper, the design and fabrication of a 3 dB Wilkinson power divider assembly for the DCS radio band is described.

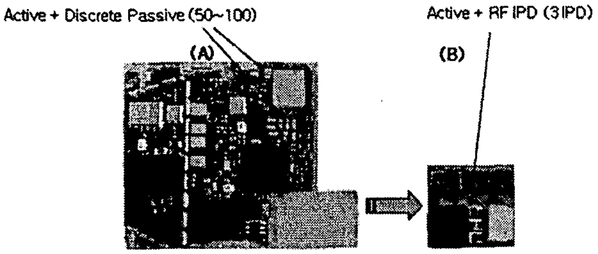

Figure 1. Digital Cellular System transceiver module using discrete passive and IPD

2. GaAs Integrated Passive Device Process

In this paper, using GaAs IPD process, in which the Wilkinson power divider circuit is implemented, used only 6 masks to realize all the design. Figure 3 presents a cross-sectional view of the GaAs integrated passive devices.

To achieve cost and size reductions, a low cost manufacturing technology for RF substrates and a high performance passive process technology was developed for RF integrated passive devices (IPDs). The fabricated substrate is a conventional 6″ GaAs wafer with a 0.5mm thickness. This substrate showed a good permittivity of 12.85, and a loss tangent of 0.006.

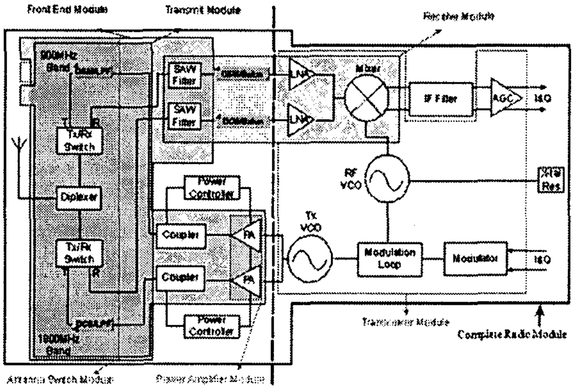

Figure 2. IPD Modern integrated GSM/DCS transceiver architecture

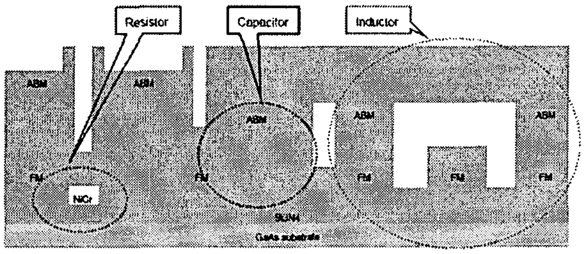

Figure 3. Cross-sectional view of the GaAs integrated passive device

The process features two levels of plated copper/gold metal with thicknesses of 5.0um (Cu 4.5um and Au 0.5um) for MET1 and 5.0um (Cu 3.0um and Au 2.0um) for MET2. All plated metals use Ti/Au seed prior to plating in order to increase the metal adhesiveness [6]. The process starts with a bottom passivation layer is composed of silicon dioxide and is deposited by plasma enhanced chemical vapor deposition (PECVD) to a thickness of 2000 Å with permittivity of 7.5, and a loss tangent of 0.002. And then a deposition of 320 Å of NiCr metallization used for thin film resistors. This transition metal alloy exhibits a wide range of resistivity, low temperature coefficient of resistance (TCR) of +80 to -250 × 10−6/°C and high stability of electrical properties and the resistivity of the refractory metal is 50Ω/☐ and is reactively evaporated. One sigma variation of the resistor values is 10% [7]. The variation depends on the width and length of the resistors and wider and longer resistors exhibit smaller variations. After evaporating NiCr, conventionally a use of Cu/Au (Cu 4.5um and Au 0.5um) MET1 is used as the contact metallization for NiCr resistors. And in this case, the Cu/Au also as the 1st metal layer for both the MIM capacitor and the spiral inductor. The reason why use copper is copper has a higher conductivity and is less expensive compared to gold. Also, copper is easily solder-able. After patterning the resistors and the lower metal part of capacitor / inductor with reactive ion etch, 2000 Å of PECVD is deposited as the capacitor middle dielectric part. After a 2000 Å deposition, an air-bridge photo process is performed prior to Cu/Au (Cu 3um and Au 2um) MET2 definition and plating. Capacitors formed with MET1 bottom plate and MET2 top plate and a dielectric result in density of 650 pF/mm2 and breakdown voltage more than 70 V and inductors consist of the 5um Cu/Au metal rings and underpass of a stack of MET1 and MET2. In final, all components are passivated with a final silicon dioxide dielectric.

3. Wilkinson Power Divider Design

The core part of power divider circuit design is λ/4 transmission lines. And it would be preferable to use lumped-element equivalent networks replacing it. In this design, a "π" lumped-element equivalent network was used. In particular, a quarter-wave line at a frequency f_o, with characteristic impedance Z_o, can be replaced for a "π" LC equivalent network as shown in Figure 4(a). The element values are given by the following equations:

$$C_P = \frac{1}{2\cdot\pi\cdot f_o} \tag{1}$$

$$L_S = \frac{Z_o}{2\cdot\pi\cdot f_o} \tag{2}$$

By replacing both λ/4 line sections by equivalent LC networks, it is possible to obtain a lumped element version of the Wilkinson divider, as shown in Figure 4(b). As noted above, this network is equivalent to the original only at the center frequency f_o. Consequently, the expected performance (insertion loss, return loss, isolation, etc.) should be similar to that exhibited by the distributed form power divider for a narrow bandwidth centered in f_o, wide enough for most applications.

The basic power divider topology is shown in Figure 5, which was designed for application to DCS band (1710-1880 MHz). This design had output impedance of 50 ohms using shunt blocking capacitor and wirebonds to the input and output pads, respectively; C1,2,3,4/L1,2 are used for "π" LC network and the balancing resistor is 100 ohm.

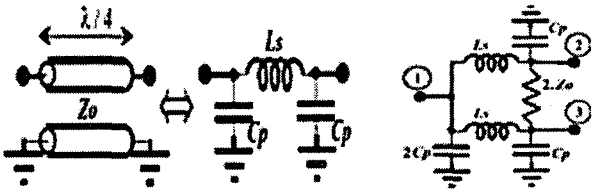

Figure 4(a). "π" equivalent network of transmission line **(b).** Schematic of lumped-element Wilkinson divider.

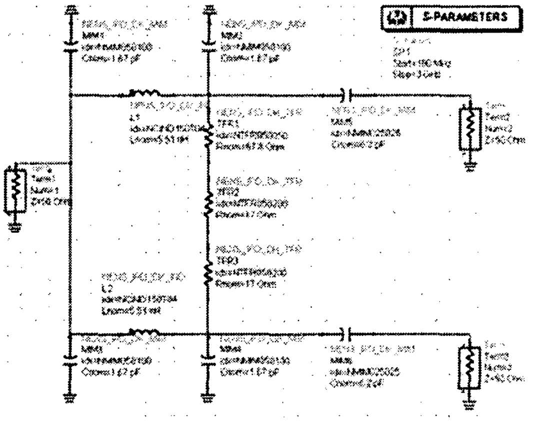

Figure 5. Topology of Wilkinson Power Divider

4. Wilkinson Power Divider Result

The Wilkinson power divider circuit as presented above is implemented in "Pi" lumped-element circuit. The detailed circuit layout on a GaAs substrate with dielectric constant 12.85 and thickness 0.5mm is shown in Figure 6. Figure 7 shows photograph of the completed 3 dB Wilkinson power divider device. The die size is about 1.52mm^2. The simulation results are superimposed in Figure 4.10 respectively. The S_{11} and S_{22} shown in Figure 4.10 represent the return loss of each ports. The S_{21} and S_{31} represent the insertion loss of the S-parameter simulation at ports 2 and 3 of the power divider from 1710MHz to 1880MHz. The S_{23} is the isolation between ports 2 and 3. During the s-parameter simulation, the frequency was swept from 0.5GHz to 3GHz. The return was larger than -20 dB. The insertion loss is less than 3.5 dB, and isolation is larger than-25 dB.

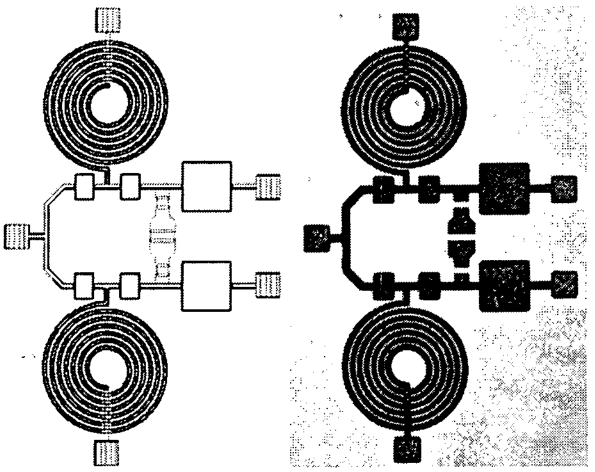

Figure 6(a). Layout of 3 dB Wilkinson power divider **(b).** Photograph of 3 dB Wilkinson power divider

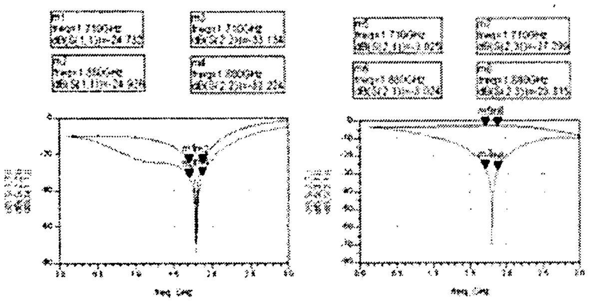

Figure 7. Simulations of return loss, insertion loss and isolation

5. Conclusion

The trend towards high integration in diverse wireless communication devices is increasing relentlessly. Integrated Passive Device Technology which was selected to design passivity on GaAs substrate shows more integrated than other topologies due to potential of compact size and used to fabricate high performance 3 dB Wilkinson power dividers for front-end modules in the DCS 1710-1880 MHz band.

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