80nm DRAM의 고압중수소 열처리에 따른 전기적 신뢰성 특성 영향

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Effect of High Pressure Deuterium post-annealing Annealing on the Electrical and Reliability properties of 80nm DRAM

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Abstract : High-pressure deuterium annealing process is proposed and investigated for enhanced electrical and reliability properties of 512Mb DDR2 DRAM without increase in process complexity. High pressure deuterium annealing (HPDA) introduced during post metal anneal (PMA) improves not only DRAM performance but also reliability characteristics of MOSFET. Compared with a control sample annealed in a conventional forming gas, additional annealing in a high pressure deuterium ambient at 400°C for 30 min decreased GIDL current and junction leakage. The improvements can be explained by deuterium incorporation at SiO_2/Si substrate interface near isolation trench edge.

Key Words : DRAM, High Pressure, Post-annealing, Reliability, Deuterium

1. 서 론

As the design rule of DRAM technology is scaled down, an ever-increasing retention time is crucial factor for high density DRAM device. Therefore, leakage reduction of a DRAM remains subjects of great interest for retention improvement, since an augmentable retention time is required as packing density increases. In order to suppress leakage current, hydrogen is used for passivating dangling bond in CMOS processing [1]. However, recently it has been reported that hydrogen treatments are degraded hot carrier immunity due to excess hydrogen [1]. Recently, passivation of interface traps by deuterium(D_2) rather than hydrogen has been reported to be an effective way to improve the hot carrier reliability of MOS devices [2-5]. In this work, Increase of data retention time to keep constant refresh interval has been investigated for the mass-productive 512Mb DRAM with 80nm feature size using high pressure deuterium annealing (HPDA).

2. 실 험

512Mb DRAM based on STI, SAC, W-bit line and MIM capacitor over-bit line (COB) structures are fabricated using boron doped (100)-oriented 8" wafers with 80nm HYNIX technologies. The key processes are listed in Table 1. After two levels of dielectric/metal interconnect process and passivation process, a 100 min H_2/N_2 anneal at 430°C is conducted finally in order to passivate the dangling bond, as shown in Fig. 1. In order to compare hydrogen annealing and deuterium annealing after FGA, HPDA (100% D_2, *10atm*) process is performed at 400°C for 30min

표1. Processing sequence of this technology

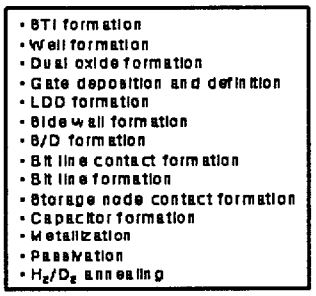
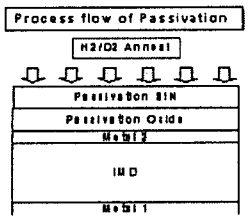


그림1. Process flow of this experiment



3. 결과 및 고찰

Samples which are annealed at high pressure deuterium ambient show increased drive current and transconductance, as shown in Fig.2 and Fig.3. However, figure 4 shows negligible change in cell Vt. Figure 5 shows slightly enhanced surface punch BV after HPDA. In Fig. 6(a), GIDL current in HPDA becomes lower than that of conventional H annealing. The reduction of leakage current is due to the decrease in interface trap density by HPDA, which has made it possible to passivate the dangling bond perfectly. The reduction of P+/N junction leakage is observed in D2-passivated sample by the same token (Fig.6(b)). D anneal sufficiently reduces the junction leakage current at the trench edge, as shown in field edge BV of Fig.7. In addition, standard deviation of field edge BV is reduced. Accelerated hot carrier DC stress measurements are performed on NMOS

at peak substrate current condition. Fig. 8(a) shows hot electron degradation lifetime versus substrate current. In Fig. 8(a), it is demonstrated that the benefits of the deuterium anneal are still observed even if the PMA is followed by a passivation caps process. After hot carrier stress with 30s, reduced threshold voltage shift was also observed in Fig. 8(b). It is clear that hot carrier lifetime is improved using HPDA-PMA.

그림2. Increased saturation drain current after HPDA.

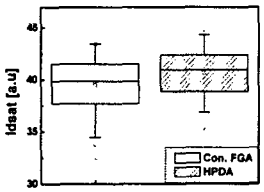


그림3. Drain current (Id) and transconductance (gm) as a function of gate voltage (Vg).

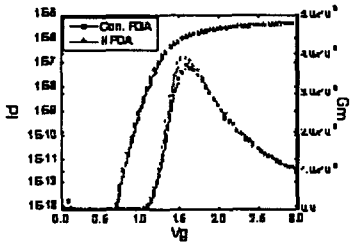


그림4. No change of cell Vt after HPDA.

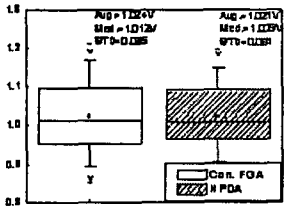


그림5. Cumulative distribution of surface punch BV.

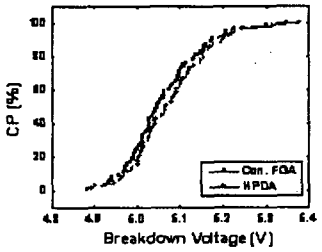


그림6. (a) GIDL current as a function of the gate voltage. (b) P/N junction leakage as a function of measurement voltage.

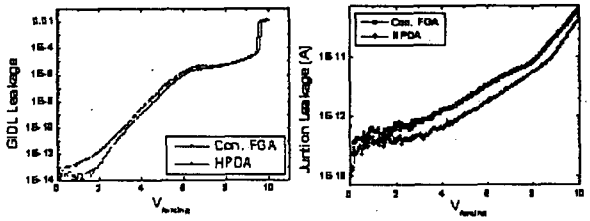


그림7. Improvement of field edge breakdown voltage after HPDA.

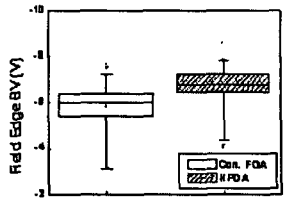


그림8. (a) NMOS hot electron lifetime versus substrate current for samples processed up to two levels of metallization including passivation dielectric. (b) Shift of PMOS threshold voltage after source experiences hot carrier stress.

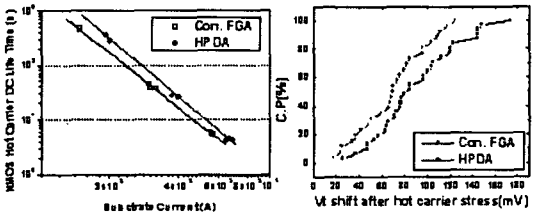


그림9. Data retention characteristics for 512Mb DRAM.

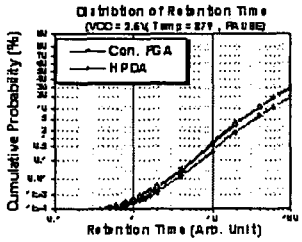


Figure 9 shows the distribution of data retention time for 512Mb DRAM. Tref of tail distribution (10^{-4} cumulative failure) is improved by 15-20% using HPDA. Moreover, it is found that pause characteristics enhance not only main but also tail distributions. Retention time improvement is attributed to the decrease of junction leakage.

4. 결 론

High-pressure deuterium annealing process is proposed and investigated for enhanced retention time characteristics of 512Mb DDR2 DRAM without increase in process complexity. The benefit of high pressure deuterium anneal may also be applicable to PMA to improve device reliability and data retention time. The improvements can be explained by deuterium incorporation at SiO_2/Si substrate interface near isolation trench edge. Therefore, high-pressure D_2 annealing shows some promise for future high density DRAM

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