SiGe-Si-SiGe 채널구조를 이용한 JFET 시뮬레이션

박병관, 양하용, 김택성, 심규환
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Simulation of Junction Field Effect Transistor using SiGe-Si-SiGe Channel Structure

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Abstract : We have performed simulation for Junction Field Effect Transistor(JFET) using Silvco to improve its electrical properties. The device structure and process conditions of Si-control JFET(Si-JFET) were determined to set its cut off voltage and drain current(at Vg=0V) to -0.5V and 300㎂, respectively. From electrical property obtained at various implantation energy, dose, and drive-in conditions of p-gate doping, we found that the drive in time of p-type gate was the most determinant factor due to severe diffusion. Therefore we newly designed SiGe-JFET, in which SiGe layer is to epitaxial layers placed above and underneath of the Si-channel. The presence of SiGe layer lessen the p-type dopants(Boron) into the n-type Si channel the phenomenon would be able to enhance the structural consistency of p-n-p junction. The influence of SiGe layer will be discussed in conjunction with boron diffusion and correspondingI-V characteristics in co -mparison with Si-control JFET

Key Words : SiGe, JFET, Silvaco