

나노선 기반 논리 회로의 이차원 시뮬레이션 연구

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Two-dimensional numerical simulation study on the nanowire-based logic circuits.

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Abstract : One-dimensional (1D) nanowires have been received much attention due to their potential for applications in various field. Recently some logic applications fabricated on various nanowires, such as ZnO, CdS, Si, are reported. These logic circuits, which consist of two- or three field effect transistors(FETs), are basic components of computation machine such as central process unit (CPU). FETs fabricated on nanowire generally have surrounded shapes of gate structure, which improve the device performance. Highly integrated circuits can also be achieved by fabricating on nano-scaled nanowires. But the numerical and SPICE simulation about the logic circuitry have never been reported and analyses of detailed parameters related to performance, such as channel doping, gate shapes, souce/drain contact and etc., were strongly needed. In our study, NAND and NOT logic circuits were simulated and characterized using 2- and 3-dimensional numerical simulation (SILVACO ATLAS) and built-in spice module(mixed mode).

Key Words : nanowire, simulation, logic, mixed mode

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