나노급 CMOSFET을 위한 Pd 적층구조를 갖는 열안정 높은 Ni-silicide

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Thermal Stable Ni-silicide Utilizing Pd Stacked Layer for nano-scale CMOSFETs

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Abstract : Silicide is inevitable for CMOSFETs to reduce RC delay by reducing the sheet resistance of gate and source/drain regions. Ni-silicide is a promising material which can be used for the 65nm CMOS technologies. Ni-silicide was proposed in order to make up for the weak points of Co-silicide and Ti-silicide, such as the high consumption of silicon and the line width limitation. Low resistivity NiSi can be formed at low temperature (~500℃) with only one-step heat treat. Ni silicide also has less dependence of sheet resistance on line width and less consumption of silicon because of low resistivity NiSi phase. However, the low thermal stability of the Ni-silicide is a major problem for the post process implementation, such as metalization or ILD(inter layer dielectric) process, that is, it is crucial to prevent both the agglomeration of mono-silicide and its transformation into $NiSi_2$. To solve the thermal immune problem of Ni-silicide, various studies, such as capping layer and inter layer, have been worked.

In this paper, the Ni-silicide utilizing Pd stacked layer (Pd/Ni/TiN) was studied for highly thermal immune nano-scale CMOSFETs technology. The proposed structure was compared with Ni/TiN structure and showed much better thermal stability than Ni/TiN.

Key Words : Pd/Ni/TiN stacked layer, Ni-silicide, thermal stability, nano-scale CMOSFETs

감사의 글

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