Downscaling of self-aligned inkjet printed polymer thin film transistors

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Keywords : Organic thin film transistors, High resolution inkjet printing

Abstract

We demonstrate here a self-aligned printing approach that allows downscaling of printed organic thin-film transistors to channel lengths of 100 – 400 nm. A perfected down-scaled polymer transistors (L= 200 nm) showing high transition frequency over 1.5 Mhz were realized with thin polymer dielectrics, controlling contact resistance, and minimizing overlap capacitance via self-aligned gate configuration.

1. Introduction

Many research groups in different scientific and technological fields to explore the potential of adapting graphic art printing techniques to the manufacturing of functional devices and structures. The vision of many of these approaches is to integrate advanced functionalities other than graphic information into large-area substrates, such as flexible paper, plastic or large-area rigid glass at a manufacturing cost that is much lower than what could be achieved with more conventional manufacturing techniques. This vision has been well articulated, but there is a range of difficult technological and scientific hurdles that will need to be overcome before reliable products can be manufactured with the required performance at low cost by commercial printing techniques. One of the key limitations at present is that the graphic arts printing equipment and printing processes need to be improved and adapted in order to meet the rather strict design rules for electronic circuits. Typical resolution capability of standard offset, gravure, screen or inkjet printing is on the order of 50 - 100 μm. Clearly, these are not necessarily fundamental limitations. Higher resolution produces little benefit in how visual images are perceived by the human eye and has therefore not been a critical issue in commercial printing. However, many applications of printed transistors require small critical feature size and line width in order to achieve adequate circuit switching speed, to minimize parasitic capacitances and undesired cross talk, or to be able to achieve the required integration density. Here we introduce fully downscaled polymer transistors via the self-aligned inkjet printing technique enabling a high resolution pattering up to 50 nm. Newly developed many other processes or techniques are integrated in the tiny transistors such as crosslikable polymer thin gate dielectrics.

3. Results and discussion

Corning 7059 glass slides were used as substrates after cleaning sequentially in an ultrasonic bath with deionised (DI) water, acetone and isopropanol. After formation of the first electrode by inkjet printing of a gold colloidal ink or conventional photolithography, the gold surface was modified by 1H, 1H, 2H, 2H-perflourodecanethiol (PFDT, Fluorochem Ltd. UK) to achieve SAP. The gold nanoparticle ink was obtained from Harima Co. Ltd. A home built inkjet printing setup with a standard single-nozzle, drop-on-demand piezoelectric print head (Microdrop GmbH, Germany) was used. The gold electrodes were then sintered on a hot plate (250 ^{o}C, 1 hour). The source/drain electrodes of some poly(9,9-dioctylfluorene-*co*-bithiophene) (F8T2) device were subsequently modified by another

SAM to improve the charge injection. The semiconducting polymer, F8T2 (Dow Chemical Company) or poly(2,5-bis(3-alkylthiophen-2yl)thieno[3,2-b]thiophene (pBTTT, Merck Chemicals) and gate insulating polymer, i.e., PMMA were spin coated on top of that in sequence. The device was completed by inkjet printing of gate electrode.

Self-aligned printing (SAP) is a bottom-up, direct-write printing technique, that is capable of defining sub-100 nm critical features with two simple additive printing steps using standard inkjet printing equipment without the need for any lithography or precise relative alignment.[1] The method comprises the steps of (a) inkjet printing a first conductive pattern onto the substrate, (b) selectively modifying the surface of the first conductive pattern to be of low surface energy without modifying the surface of the substrate, and (c) inkjet printing a second conductive pattern partially overlapping with the first conductive pattern, but not requiring precise relative alignment (Fig. 1a). The droplets of the second pattern are repelled by and flow off the low-energy surface of the first pattern and dry with their contact line in close proximity to the edge of the first pattern, but forming a small self-aligned, electrically insulated gap. The size of this gap is not defined by any top-down patterning step as in previous approaches, but is entirely controlled by the dynamics of the contact line motion when the droplets flow off the surface of the first electrode. The SAP technique is a scalable nano patterning technique for critical feature definition with high patterning yield (as tested on arrays of several 1000 TFTs), and provides a route to much higher circuit switching speed than what is currently possible with standard graphic arts printing techniques. In our original work we used conducting polymers to fabricate SAP electrodes. In this case the physical channel length was found to be limited by the relatively low conductivity of the conducting polymer (typically 1-10 S/cm) leading to significant voltage drops near the edge of the channel.[2] We report Here on the realization of highly conductive nanoelectrodes with gap dimensions of 60-200 nm using gold nanoparticle inks (Fig 1b).

One of the most important requirements for a submicrometer TFT is a gate dielectric layer that can be made sufficiently thin to meet basic scaling requirements. Insufficient scaling of gate dielectric thickness leads to severe degradation of device performance due to short-channel effects, such as loss

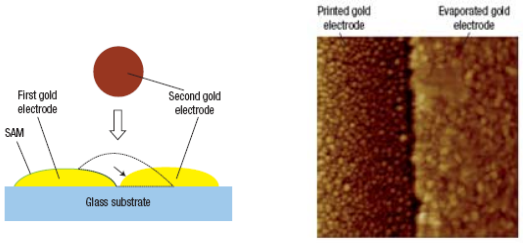

Fig. 1. (a) Principle of self-aligned printing technique. (b) Atomic force micrograph of Au source/drain electrodes with sub-100 nm channel length fabricated by SAP.

of current saturation as seen in our previously reported SAP devices.[2] Several research groups have reported robust crosslinkable polymers with low free volume as thin gate insulators (> 15 nm) in bottom-gate structure.[3] There are problems to apply these to the top gate architecture needed here including a high curing temperature (typically over 150 °C for 30 minutes) resulting in damage to the underlying semiconductor film and the need to use an orthogonal solvent that avoids swelling and dissolution of the underlying semiconducting polymer. To overcome these we selected a crosslinked polymer blend gate dielectric with poly(methyl methacrylate) (PMMA) as a base polymer and 1,6-bis(trichlorosilyl)hexane as a

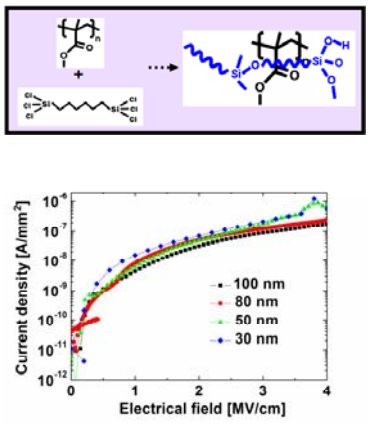

Fig. 2. (a) Chemical structure of poly(methyl methacrylate) (PMMA) and crosslinker (left side) and crosslinked PMMA (C-PMMA, right side). (b) Leakage current density versus applied voltage of C-PMMA polymer films sandwiched between gold

electrodes.

crosslinker (C-PMMA) in n-butyl acetate orthogonal solvent (Fig. 2a)[4].

The main advantage of this system is that the crosslinking takes place at room temperature spontaneously in the presence of oxygen and moisture in air. Comparing a number of different base polymers including poly(styrene) or poly(hydroxylstyrene) PMMA exhibited the best results with a high breakdown strength (>3 MV/cm) and a low leakage current (10 – 100 nA/mm^2 at 2 MV/cm) for gate dielectric thickness d down to 30 – 50 nm. This performance is comparable to that of thermal SiO_2 on Si (Fig. 2b). The leakage current is low enough to permit operating the device at high frequency and further reducing is expected via patterning semiconductor to minimize cross-talk between transistors. Using the semiconducting polymer poly(dioctylfluorene-co-bithiophene) (F8T2) and a C-PMMA gate dielectric this allowed fabrication of fully downscaled printed TFTs operating at voltages below 5 – 8 V.

In order to remain compatible with large-area manufacturing it is important that not only the channel length, but the entire device structure is defined in a self-aligned manner. We have developed a self-aligned gate architecture to minimize the parasitic overlap capacitances, C_{gs} and C_{gd}, that would otherwise be associated with the 50 – 100 μm wide printed gate line overlapping with the source and drain electrodes. With state-of-the-art volume printing on large-area flexible substrates it is presently not possible to significantly reduce linewidths due to the difficulties of dispensing small liquid volumes nor is it possible to align precisely gate and source/drain patterns with respect to each other. This leads to undesirably large and variable C_{gs} and C_{gd} and is one of the key reasons for the poor TFT performance reported in the literature[5]. The fabrication process of our self-aligned gate structure comprises the steps of i) depositing a thick (1 μm), second UV photosensitive dielectric layer (Shipley 1813 positive UV photoresist) on top of the thin (30 – 50 nm) gate dielectric layer, (ii) irradiating the structure with light through the back of the substrate to selectively expose the channel region with the optically opaque source and drain electrodes acting as a shadow mask, iii) developing the photoresist into a trench structure self-aligned with respect to the edges of the source and drain electrodes, and (iv) depositing a wide gate electrode by inkjet printing. In this structure the overlap capacitance is minimized in spite of the wide printed linewidth. The gate dielectric is thin only over the channel where this is wanted and the overlap capacitance becomes insensitive to variations of the position of the gate electrode (Fig. 3a).

Figure 3b shows cross-sectional SEM images of a test structure in which the first source-drain electrode was defined by photolithography, and the second SAP electrode was inkjet printed. Interestingly, we found that the overlap of the trench with the printed gold electrode (~ 1 μm) was larger than the overlap with the photolithographically defined electrode (200 ~ 300 nm). The printed electrode has a smooth thickness profile dropping continuously to zero near its edge, and as a result some light passes through it in the vicinity of the edge leading to a small widening of the trench structure on the side of the printed electrode. This is desirable because it provides a method for controlling the source/drain-to-gate overlap length with the edge profile of the printed electrode. As discussed above it is in fact not desirable to have strictly zero overlap length in a submicrometer, self-aligned gate OTFT since this would put very stringent limitations on the injection of charges from the source-drain contacts into the channel. In the presence of a small, but finite overlap length contact resistance effects can be minimized by current crowding while maintaining a small overlap capacitance. The overlap capacitance between a printed PEDOT:PSS gate and a lithographically defined gold source/drain electrode was measured to be 0.1 – 0.3 pF/mm. Consistent with the FIB-SEM measurements the overlap capacitance between PEDOT:PSS gate and the printed gold source/drain electrode is slightly higher (0.6 – 0.8 pF/mm). These values are at least a factor of 5 – 10 lower than that of reference devices without the self-aligned gate structure (Fig. 3c). The self-aligned device architecture is compatible with high-mobility, state-of-the-art polymer semiconductors, such as F8T2 or poly(2,5-bis(3-alkylthiophen-2yl)thieno[3,2-b]thiophene (pBTTT).

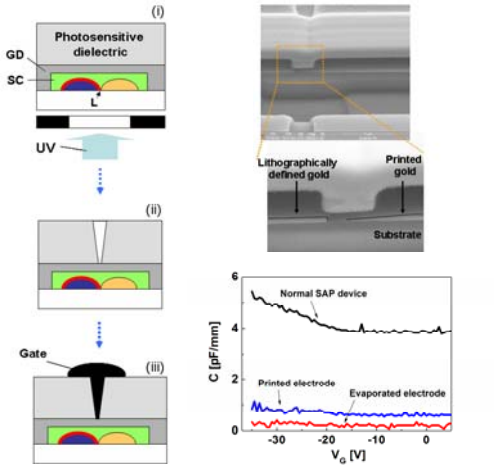

Fig. 3. a, Schematic outline of the process to form SAG structure (b) Cross-sectional view of SAG structure measured by focused ion beam scanning electron microscopy (FIB-SEM). (c) Capacitance-voltage characteristics of F8T2/C-PMMA FET with self-aligned printed source-drain electrodes and unconfined PEDOT:PSS top-gate electrodes (black line).

No degradation in device performance during the UV photo-exposure and the subsequent trench development step in alkaline developer was observed with pBTTT or F8T2 and 30 nm C-PMMA gate dielectric. Using pBTTT we have realized high-performance self-aligned devices operating below 5-8 V with mobilities of 0.1 ~ 0.2. To estimate the switching speed which could be achieved with such devices we have measured the transition frequency f_T of the discrete transistors in a number of different configurations (Fig. 4). f_T is determined as the cross-over point at which the AC modulated channel current in response to a gate voltage modulation becomes equal to the parasitic current flowing through the gate-to-source/drain capacitance. The combination of shortening of the channel by SAP and the higher mobility of pBTTT (pBTTT SAP) results in a significant improvement compared to standard micron scale F8T2 device (F8T2 L = 5 m), but the transition frequency remains limited to relatively small values of 40 kHz. However, the self-aligned gate architecture allows reducing the parasitic current through the gate significantly while retaining a high transconductance / channel current modulation, and achieving f_T values around 1.6 MHz (pBTTT SAG).

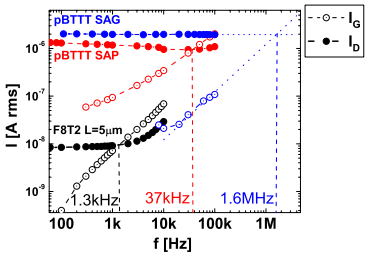

Fig. 4. Root mean square value of drain (filled circles) and gate (hollow circles) currents versus frequency of a micro channel length F8T2 transistor (black; L = 5 μm W = 1 mm), a SAP pBTTT transistor (red; L ≈ 200 nm, W = 500 μm) without SAG and a SAP pBTTT transistor with SAG (blue; L ≈ 200 nm, W = 500 μm).

4. Summary

We have developed a printing process for submicrometer polymer TFTs that allows meeting basic scaling requirements for downscaling and at the same time remains compatible with the manufacturing requirements for large-area, flexible electronics.

5. References

1. Y.-Y. Noh, N. Zhao, M. Caironi, and H. Sirringhaus, Nature Nanotechno. **2**, 784 (2007).
2. C. W. Sele et al., *Adv. Mater.* **17**, 997 (2005).
3. L. L. Chua, *et al. Nature* **434**, 194 (2005).
4. M. H. Yoon, H. Yan, A. Facchetti, T. J. Marks, *J. Am. Chem. Soc.* **127**, 10388-10395 (2005).
5. H. Sirringhaus *et al. Science* **290**, 2123 (2000).