# LED Driver Solution for Backlighting large TFT-LCD Panels with Adaptive Power Control & Video Synchronization

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## Abstract

*mSilica developed a scalable integrated circuit solution for driving multiple arrays of LEDs to backlight TFT-LCD panels. The drivers incorporate adaptive power control of the DC-DC power supply powering the LEDs to improve the efficiency while synchronizing PWM dimming with video timing signals VSYNC and HSYNC to reduce motion blur.*


## Introduction

In recent years there has been high interest in using LEDs for backlighting TFT-LCD panels to (i) improve contrast ratio (ii) reduce motion blur and (iii) reduce power consumption. Several techniques for increasing power savings while simultaneously improving contrast ratio and reducing motion blur have been proposed with progressive dimming improvements, 0, 1, and 2 dimensional (0D, 1D, 2D) backlight unit configurations [1]. Previous implementations of LED drivers had expensive individual string power control of LEDs without a serial interface for implementing dimming improvements [2]. mSilica's driver technique incorporates decentralized adaptive voltage scaling and synchronization to video timing signals in a single integrated circuit. Refer the block diagram in Figure 1.

mSilica evaluated a circuit with 16 series LED strings of 10 OSRAM LW_G6SP white LEDs per string driven at 100mA. A typical 47" LCD TV with full HD 1080P display and 2D dimming control would have 128 such LED strings. The evaluated circuit represents a portion of the total backlight for this panel. Some aspects of the driver have been described before [4].

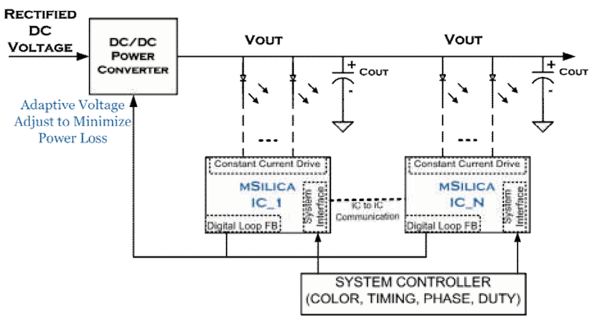


**Fig 1. System Implementation of the Adaptive Power Control and Video Synchronization**

Depending on the LED forward voltage ($V_F$) bin the series LED string voltage varies from 29V to 41V as shown in table 1 [3]. Typically LCD TV manufacturers design the PSU for LEDs with the worst case, $V_{F,}$ to ensure all strings maintain regulation under all conditions.

**Table 1. Vf bins for OSRAM LW_G6SP LEDs**

Durchlassspannungsgruppen[6) Seite 17]
Forward Voltage Groups[6) page 17]

| Gruppe Group | Durchlassspannung Forward voltage min. | Durchlassspannung Forward voltage max. | Einheit Unit |
|---|---|---|---|
| 4 | 2.9 | 3.2 | V |
| 5 | 3.2 | 3.5 | V |
| 6 | 3.5 | 3.8 | V |
| 7 | 3.8 | 4.1 | V |

LED strings are binned to ensure that the Vf mismatch of the string (not individual LEDs) is within ±2V.

**LED Control and Decentralized Adaptive Power Scaling[1]:**

The technique of decentralized power regulation involves mixed-signal processing to adaptively control DC-DC power supply unit (PSU) that provide input power to LED strings. Figure 2 shows the schematic representation of the mSilica driver integrated circuit.

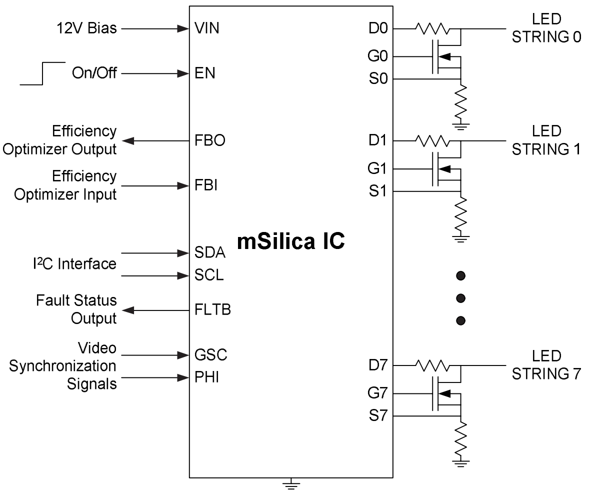


**Fig 2. Schematic of mSilica LED Driver IC**

Each mSilica driver controls eight separate series LED strings with a constant current sink maintained within 2% of target current. Particularly of interest for adaptive PSU control are signals FBO (Feedback Output) and FBI (Feedback Input). The separate DC/DC PSU sets the initial output voltage, which is the worst case series LED string forward voltage plus current sink headroom.

In the presented example, the initial voltage is determined to be approximately 42V based on the Vf bins shown in Table 1 and according to the following equations:

$$V_{OUT(MAX)} \geq V_{LEDx(MAX)} + V_{FETx(MIN)} + R_{SENx} \qquad (1)$$

$$V_{OUT(MIN)} \leq V_{LED(MIN)} + V_{FET(MIN)} \qquad (2)$$

[1] Patents Pending

$V_{OUT(MAX)}$ and $V_{OUT(MIN)}$ numbers must also account for initial accuracy and drift of the PSU itself.

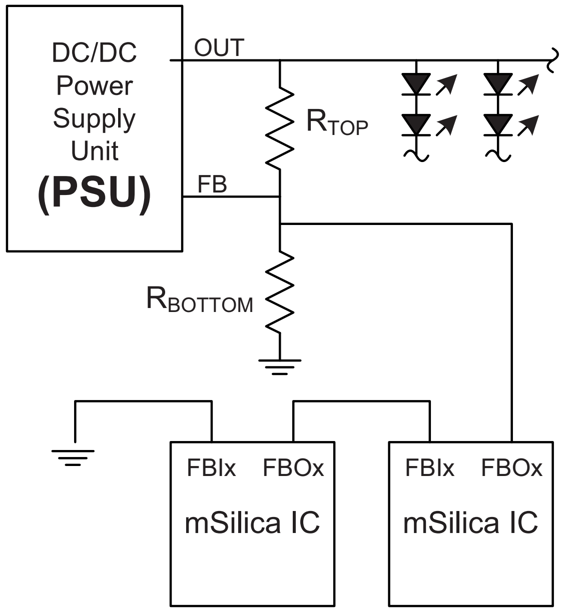


**Fig 3. Adaptive PSU control concept**

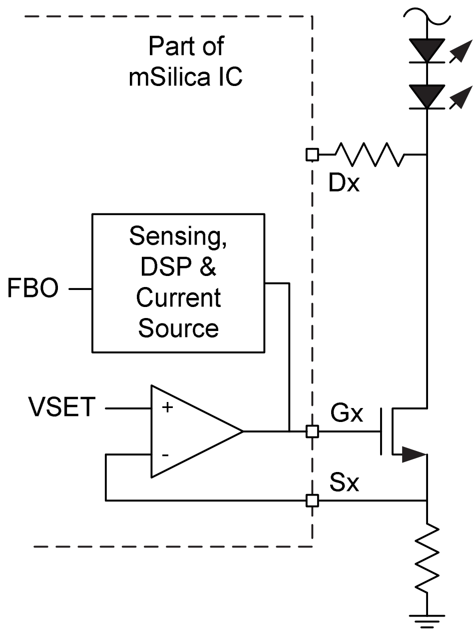


**Fig 4. Feedback mechanism for adaptive PSU control**

To minimize MOSFET losses, the sensing circuitry continuously monitors the MOSFET gate voltage and detects if the MOSFET has sufficient drain voltage to maintain LED current regulation. If the sensing circuitry determines that the MOSFET is not in the operating region, unable to maintain current regulation, it reduces the PSU output using a digital signal processing algorithm. Adaptive control is achieved by injecting a current to PSU voltage divider to reduce the power supply output voltage.

At initial turn-on, after the power supply voltage stabilizes, the IC begins reducing the voltage until insufficient drain voltage is detected on any LED string powered by that PSU, at which time it increases the power supply voltage by two steps. The driver continues to monitor the MOSFET and if it detects insufficient voltage, it increases the PSU voltage. This configuration allows for the lowest voltage possible at the MOSFET drain while maintaining accurate LED current regulation on all the strings. The configuration also allows the driver to adapt to continuously changing LED string voltage drops due to aging, temperature changes and PSU voltage drift. An additional benefit of this approach, due to the fact that the delay between PSU output voltage adjustments is greater than the PSU settling time, is that the output voltage control system does not interact with the PSU regulation loop, preventing loop interaction which could result in unstable behavior. The following waveform illustrates the adaptive scaling.

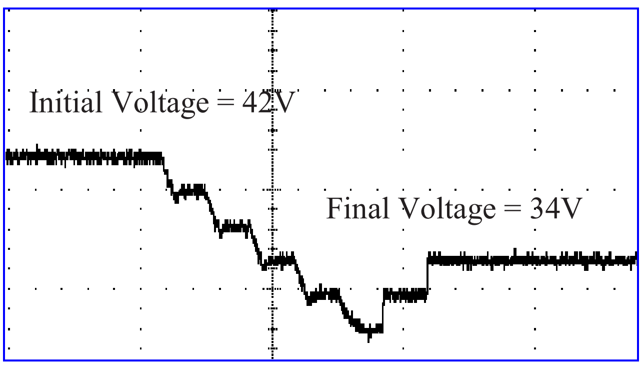


**Fig 4. Adaptive voltage scaling waveform**

The driver allows for adjusting:

(i) Step size to cover the required voltage range within a given number of steps
(ii) Step duration corresponding to the DC/DC PSU settling time
(iii) Number of steps to program the LED voltage headroom

Additionally, multiple drivers can be cascaded as shown in figure 3, thus providing a scalable, decentralized adaptive voltage scaling solution. The example circuit yielded approximately 20% reduction of power at initial turn-on as seen in figure 4. During operation, there was more power reduction as the driver adjusted to decreasing LED $V_F$ due to LED self heating and the negative temperature coefficient of LED $V_F$.

## Contrast Ratio improvement and Motion Blur Reduction

The mSilica driver controls LED brightness using PWM dimming synchronized with the video frame timing (VSYNC) as well as the horizontal lines refresh timing (HSYNC) to easily implement both 'scanning' and 'blinking' type solutions, to reduce motion blur and enhance contrast ratio. The following block diagram shows the LED driving and dimming engine.

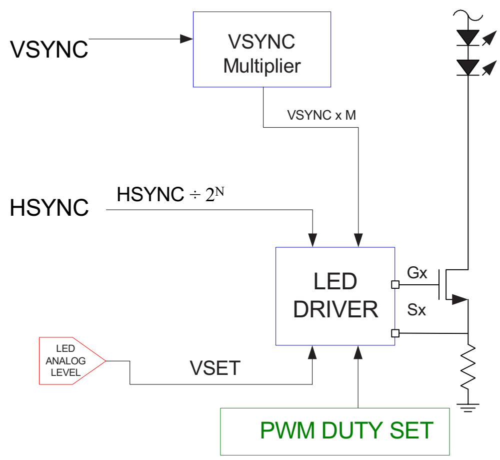


**Fig 5. Block diagram of video synchronized LED driving and dimming engine**

With the ability to turn off the section of the Backlight Unit (BLU) behind video lines that are being refreshed allows the system to reduce motion blur, and thereby reduce backlight power as the backlight is turned off during the short periods that the screen is being refreshed. This ability to synchronize to the video clocks gives the system designer the ability to blank different portions of the BLU at periods synchronized to the LCD panel refresh timing to apply 2- and 3-d regional dimming thereby further reducing power consumption in the BLU.

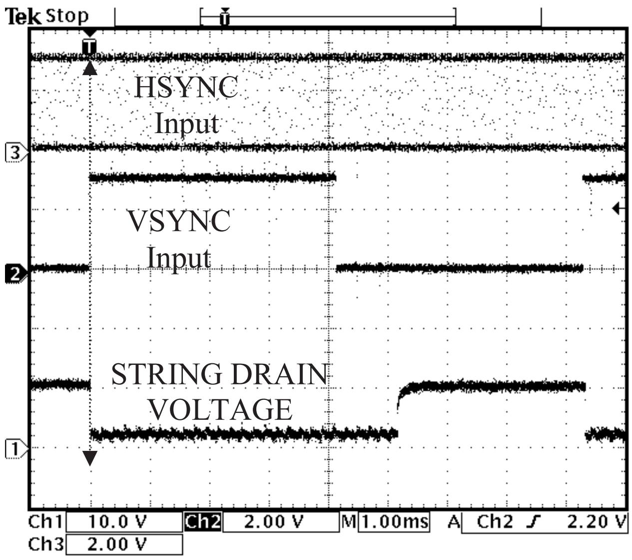


**Fig 6. Synchronized LED driving with VSYNC and HSYNC rising edge**

Each series LED string has an independent on-time. Each string also had an independent delay with respect to, and frequency equal to, the VSYNC signal. The on-time is set as number of HSYNC pulses, and is calculated as the product of the driver PWM register value for that string and the global intensity register value. Each string is turned on after the VSYNCH signal edge a number of HSYNC pulses as set by the driver internal phase delay register for that string.

This technique allows the LED brightness to be adjusted individually for white point color control and for regional dimming. When used in a "tiled" direct backlighting scheme, this not only allows frame-by-frame regional control of brightness and color thereby improving the available color saturation and contrast of the LCD panel but also blanks the panel during each VSYNC refresh thus reducing motion blur along with reducing backlight power consumption for improved power efficiency.

Independent phase delay with respect to the frame refresh rate allows each region to be turned off while lines of that region are being updated to reduce the unwanted motion blur artifacts as well as reducing power dissipation. Another benefit to synchronizing the PWM dimming to the frame refresh rate is that it eliminates "waterfall" noise. Waterfall noise is caused by crosstalk of signals that produce a low-frequency beat that manifests visible artifacts that slowly propagate up or down the LCD panel.

## Summary

A new system-centric LED driver integrated circuit was developed for large TFT-LCD panel backlighting. Two important aspects of the backlight system, adaptive power control of the input DC-DC PSU and synchronization to video signals was studied. While the adaptive power control allowed for over 20% power saving in our studied, the synchronization of LED string PWM to the VSYNC and HSYNC was proposed to reduce motion blur and eliminate waterfall noise.

## References

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