Top gate ZnO-TFT driving AM-OLED fabricated on a plastic substrate

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Abstract

We have fabricated 2.5 inch QQCIF AM-OLED panel driven by ZnO-TFT on a plastic substrate for the first time. The number of photo mask for the whole panel process was 5 and the TFT structure was top gate with active protection layer as a first gate insulator. Optimizing the process for the substrate buffer layer, active layer, ZnO protection layer, and gate insulator was key factor to achieve the TFT performance enough to drive OLED. The ZnO TFT has mobility of 5.4 $cm^2/V.s$, turn on voltage of -6.8 V, sub-threshold swing of 0.39 V/decade, and on/off ratio of $1.7x10^9$. Although whole process temperature is below 150°C to be suitable for the plastic substrate, performance of ZnO TFT was comparable to that fabricated at higher temperature on the glass.

1. Introduction

As people want to implement thinner and lighter display, research interests in a display on a plastic substrate have been increased. Recently, there have been many efforts to make AM display on a plastic substrate using a-Si TFT and organic TFT.[1,2] One of the successful things was AM-OLED driven by organic TFT demonstrated by SONY last year.[3] The total process, however, seems to be very complex and simple process would be essential for the plastic display to be viable in the real market.

Oxide TFTs which can be fabricated at relatively low temperature by simple process with moderate performance are considered to be good candidates for the flexible display.[4,5] AM-OLED driven by IZGO TFT on a metal substrate was demonstrated in 2007 by LGE.[6] However, the process temperature was as high as 350°C and it is too high to carry out on a plastic substrate.

Here, we report on the ZnO TFT driving AM-OLED fabricated on a plastic substrate for the first time. We used just 5 photo-masks for the whole backplane processes and they were carried out at lower than 150 °C. This shows the promise of ZnO TFT for the plastic display.

2. Experimental

In a fabrication of backplane on a plastic substrate, the alignment of each layer of TFT is one of the most difficult things to solve. Pre-treatment of substrate which makes it shrink enough before starting the TFT process is one of the most important methods to avoid misalignment of each layer. We annealed arylite substrate in a 200°C vacuum oven for 48 hours and substrate was attached on a 5" Si wafer using the adhesive. The substrate buffer layer, alumina, was deposited on an arylite attached to the Si wafer in 30nm thickness.

For the fabrication of backplane, source/drain (S/D) consisted of three layers of Al/Cr/IZO was deposited on the alumina buffer layer. After patterning of S/D electrode by wet process, ZnO semiconductor films were deposited by means of PEALD at the RF power of 130W at 150 °C and ZnO protection layer (PL) was deposited by ALD.[7] After patterning ZnO and PL using diluted acid at once, alumina was deposited at the temperature of 120°C by means of ALD, followed by S/D electrode pad opening by wet etching of alumina. Sputtered Al/Cr bi-layered film was used as a gate electrode as well as OLED anode and patterned by wet process. OLED bank was formed by conventional photo process and annealed at vacuum oven at 150°C. The structure of top emission OLED fabricated by vacuum thermal deposition was NPB (40 nm)/ DPVBI:BD (30 nm)/ LGET185 (30 nm)/ LiF (1 nm)/ Al (15

nm)/Ag (10nm). The structure of TFT is shown in the figure 1.

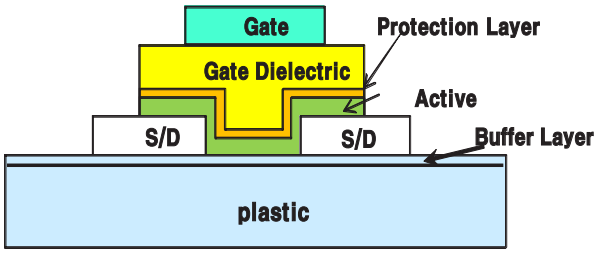

Figure 1. Schematic cross sectional diagram of ZnO TFT

3. Results and Discussion

In a fabrication of AM-OLED on a plastic substrate, selection of substrate buffer was one of the most important factors, since it played several roles, especially in a top gate TFT structure. We selected alumina film deposited by ALD as a buffer layer. The process optimization of plastic substrate buffer layer is very important for the alignment of each layer of TFT as well as the pretreatment of substrate. Without buffer layer, it was very hard to align each layer right. Figure 2 shows optical image of TFT array and align keys which show good alignment of each layer. This was obtained by pretreatment of substrate, time delayed exposure which was developed by our group previously[8], and proper selection of buffer layer.

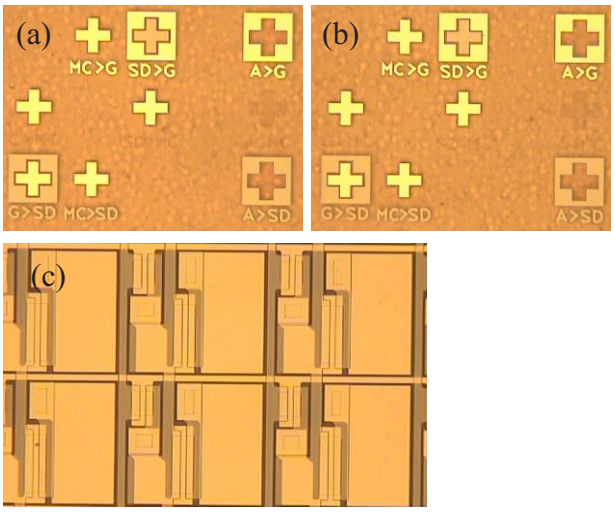

Figure 2. optical image of align keys located in a left (a) and right side (b) of 5" substrate, and TFT array (c).

The second role of substrate buffer is a protection layer from water penetration. We need high barrier layer for the substrate since OLED is very sensitive to water and oxygen. It is well known that alumina film grown by ALD has superior water barrier layer.[9] Water permeability of 30 nm thick alumina film could not be measured by MOCON since it showed the limited value of low 10^{-3}g/m^2.day. The third role of buffer layer is a formation of a back channel interface with an active layer in a top gate TFT as shown in a figure 1. In a top gate ZnO TFT, substrate buffer layer affects TFT performance significantly.[10] Therefore, optimization of buffer layer is most important when we fabricate TFT on the plastic substrate. Without mentioning that different material of buffer layer resulted in a totally different performance, even same alumina gave us different results according to the deposition temperature.

Secondly important material design was S/D layer. We adopted triple layer of Al/Cr/IZO as a S/D. IZO was used for the ohmic contact with active layer, Cr was used for the etch stopper during the gate insulator wet etching, and Al was used to gain flexibility.

As an active layer and active protection layer (PL), we used ZnO and alumina, respectively. Although a-IZGO TFTs fabricated on a glass showed excellent performance, they mostly need thermal treatment as high as 300°C. Furthermore, a-IGZO TFT array deposited on a PEN at room temperature just showed feasibility of driving e-paper.[5] Instead, ZnO grown by PEALD at the temperature as low as 150°C showed promise for the OLED backplane.[11] In addition, proper use of ZnO protection layer could improve the TFT performance.[7] Hence, we deposited ZnO layer by PEALD and alumina by ALD at 150°C, respectively.

In a selection of gate insulator, we focused on the film stress since gate insulator covers whole panel area, inducing large film stress. Inorganic dielectric layer mostly has large stress which is dependent on the process temperature. Since films on a plastic substrate could be cracked or delaminated due to the difference of CTE of each layer and stress, reducing stress is very important. However, one thing we also have to take into account is any kind of component in a gate

insulator which induces Von shift or instability of TFT. Although adopting organic dielectric layer could reduce the film stress, it contrarily resulted in poor device performance as shown in the figure 3. The devices were fabricated on a glass substrate to eliminate other factor and just to investigate the effect of organic dielectric on the device characteristics.

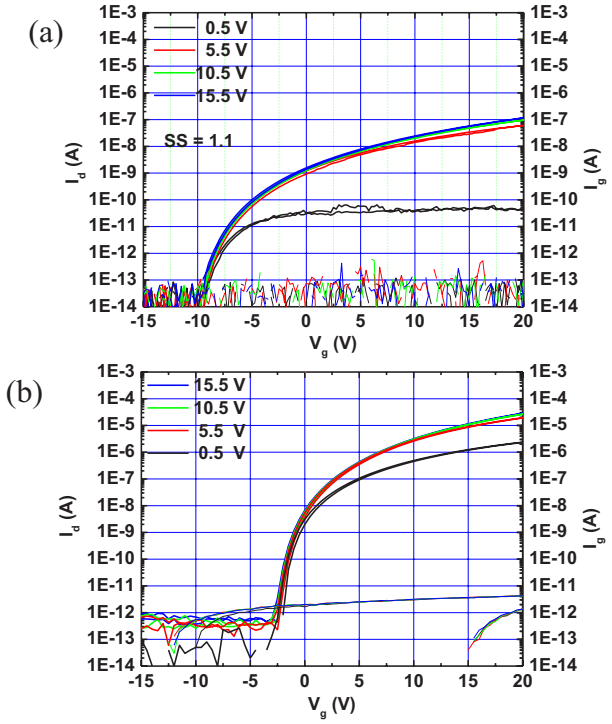

Figure 3. ZnO TFTs adopting (a) 30 nm of AlO/organic dielectric double layer (μ =0.01 cm^2/V.s) and (b) AlO single layer (μ = 4.2 cm^2/V.s) as a gate insulator. (W/L = 320μm/ 20μm)

We used alumina grown by ALD as a gate insulator and could reduce the gate insulator film stress by lowering the growth temperature. Although alumina grown by ALD even at a low deposition temperature gives low leakage current, it rather has lots of hydroxyl group. We could eliminate these by annealing during the OLED bank process.

Variation of each process temperature for the substrate buffer layer, active layer, and ZnO protection layer changed TFT performance greatly. Therefore optimizing each process temperature was the key factor to achieve good TFT performance.

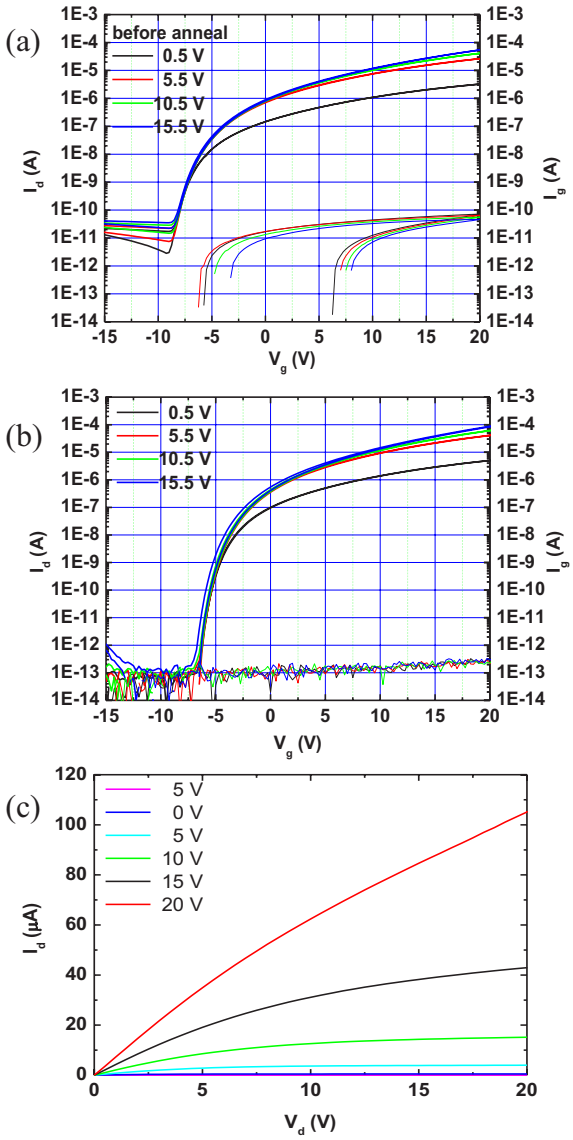

Figure 4. (a) Transfer characteristics of ZnO-TFT with a W/L=80/20 for as fabricated ZnO TFT (b) Transfer characteristics of ZnO-TFT with a W/L=80/20 for as fabricated ZnO TFT V_{DS} varying from 0.5 to 15.5V and (c) Output characteristics for a ZnO-TFT with a W/L=80/20 for V_{GS} varying from 5 to 20V. (b) and (c) were obtained after panel process finished

Figure 4 shows performance of switching TFT with the W/L dimension of 80 μm /20 μm.

Annealing array during the panel process reduced off-current, S.S value, and gate leakage current, and increased on-current. The ZnO TFT has mobility of 5.4 cm^2/V.s, turn on voltage of -6.8 V, sub-threshold swing of 0.39 V/decade, and on/off ratio of $1.7x10^9$.

Although turn on voltage is more or less negatively shifted, performance of ZnO TFT was comparable to that fabricated at higher temperature on the glass.

Figure 5 shows operating image of top emission 2.5 inch AM-OLED fabricated on a plastic. One pixel consisted of 2T/1C and driving TFT dimension is 200 μm /20 μm. This is the first demonstration of ZnO TFT driving AM-OLED fabricated on a plastic.

Figure 5. Operating image of top emission AM-OLED on a plastic driven by ZnO TTF.

Table 1. Specification of AM-OLED on a plastic

panel size	**2.5”**
resolution	**88 (scan) x 110 (data)**
pixel pitch	**430 x 470 μm^2**
aperture ratio	**27%**

4. Summary

We have fabricated ZnO TFT driving AM-OLED on a plastic substrate for the first time. Optimizing each process such as substrate buffer layer, active layer, and gate insulator was the key factor to achieve good ZnO TFT performance. Although all processes were carried out under 150°C, TFT performance was comparable to that fabricated on a glass substrate and this opens new way to the plastic display. This showed the promise of ZnO TFT for the flexible display.

5. Acknowledgements

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6. References

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