Silicon Thin-Film Transistors on Flexible Polymer Foil Substrates

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Abstract

Amorphous silicon (a-Si:H) thin-film transistors (TFTs) are fabricated on flexible organic polymer foil substrates. As-fabricated performance, electrical bias-stability at elevated temperatures, electrical response under mechanical flexing, and prolonged mechanical stability of the TFTs are studied. TFTs made on plastic at ultra low process temperatures of 150ºC show initial electrical performance like TFTs made on glass but large gate-bias stress instability. An abnormal saturation of the instability against operation temperature is observed.

1. Introduction

Flexible thin-film transistor backplanes are generic components of flexible active matrix displays [1]. In particular, silicon TFT backplane on plastic are desirable for drop-in replacement of current standard glass backplane. To make a-Si:H TFTs compatible with commercially available plastic substrates, the process temperature is usually reduced to 200°C or less. While the as-fabricated performance of the TFTs made at temperature down to 150°C is acceptable [2], their bias-stress stability is poor. In addition to being stable against electrical bias stress, on-plastic TFTs must keep functioning during and after mechanical flexing. The field-effect mobility rises in tension and drops in compression; a small change of subthreshold slope is found in a-Si:H TFTs on plastic substrate when put under short-term mechanical strain [3]. The long-term electro-mechanical stability of flexible a-Si:H TFT backplanes is a concern for reliable flexible display applications. Another important issue is the electrical-bias stress stability at elevated substrate temperature. Under frequent operation, rising of the device temperature can be significant because typical plastic substrates have low thermal conductivities. The shift of threshold voltage ΔV_t in *a*-Si:H TFTs made at a conventional process temperature of 300°C or above increases with the stressing time and the stressing [4-7], while an abnormal saturation of ΔV_t at 50°C (323K) is observed in our low-temperature processed TFTs.

2. Experimental

The a-Si:H TFTs were fabricated on 51μm thick Kapton E polyimide foil substrates at 150°C. These TFTs have the standard inverted-staggered back-channel cut structure as shown in Figure 1. Prior to TFT fabrication, the substrate is coated on both faces with a plasma-enhanced chemical vapor-deposited (PE-CVD) SiN_x layer for chemical and adhesion. The substrate is held loosely in a frame and faces downward into the glow discharge. First a sandwich structure of 10nm Cr / 100nm Aℓ / 10nm Cr is thermally evaporated and wet etched to create the gate electrode. Then we deposit the tri-layer stack of SiN_x gate dielectric / undoped a-Si:H channel / n^+ a-Si:H source-drain by PE-CVD, followed by an ~ 100 nm thick thermally-evaporated Cr layer as source-drain contact. Then the source-drain electrodes and TFT islands were defined by photolithography and dry/wet etched. Last, the gate contact hole was opened by dry etching through the gate dielectric. The gas flow ratios were $SiH_4 : NH_3 : H_2 = 1 : 10 : 44$, $SiH_4 : H_2 = 1 : 1$, and $PH_3 : H_2 : SiH_4 = 0.01 : 1 : 7$ for the SiN_x, i a-Si:H, and n^+ a-Si, respectively.

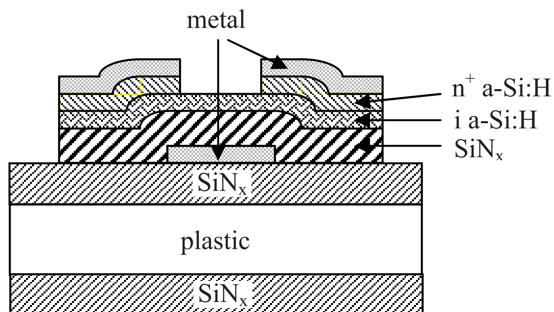

Fig. 1. Schematic cross section of a back-channel etched a-Si:H TFT on a passivated plastic substrate.

HP 4155A parameter analyzer and low-noise probes were used for I-V characterization. For the study of long-term electro-mechanical stability, the TFTs are evaluated before and after bending around cylinders of decreasing radii to set defined values of compressive or tensile strain. We apply strains up to TFT fracture. In tension a-Si:H TFTs break at about 0.3% strain, and in compression at about 2% strain. Lengthy experimentation shows that only very large strains produce measurable changes in TFT characteristics. Therefore we concentrate on applying the largest mechanical strain that can be applied without breaking the TFTs, 1.8% in compression, in the source-drain direction by bending the TFT/Kapton around a cylinder with axis perpendicular to the channel direction. For electrical evaluation the TFT is taken off the cylinder and then is mounted again for more bending, up to a total bending time of 23 days.

The electrical gate-bias stress experiments at elevated temperatures were carried out by applying 20 V to the gate while keeping the source and the drain grounded at various temperatures. The samples were heated using a thermoelectric heating stage. For each temperature, the measurements were performed after the temperature reached steady state. We extract the threshold voltage V_t at $I_{ds} = 10^{-8}$ A, the on current Ion at $V_{gs} = 25$ V, and the off current at $V_{gs} = -5$ V from the transfer curves of $V_{ds} = 10$ V.

3. Results and discussion

Long-term electro-mechanical stability

Figure 2 shows the effects of prolonged compression on the TFT parameters. All data are normalized to their initial, as-fabricated, values. Figure 2(a) shows that threshold voltage initially drops and then increases with $t^{0.10}$, while the gate leakage current decreases slightly. Figure 2(b) indicates little effect of strain on I_{on} and some reduction of I_{off}. Figure 2(c) shows that the mobility remains essentially constant, in agreement with the nearly constant I_{on}, while the subthreshold slope S decreases slightly. Within the boundaries of practicable gate bias stress and compressive stress, the mechanical stress changes V_t and I_g about 100 times slower than electrical stress.

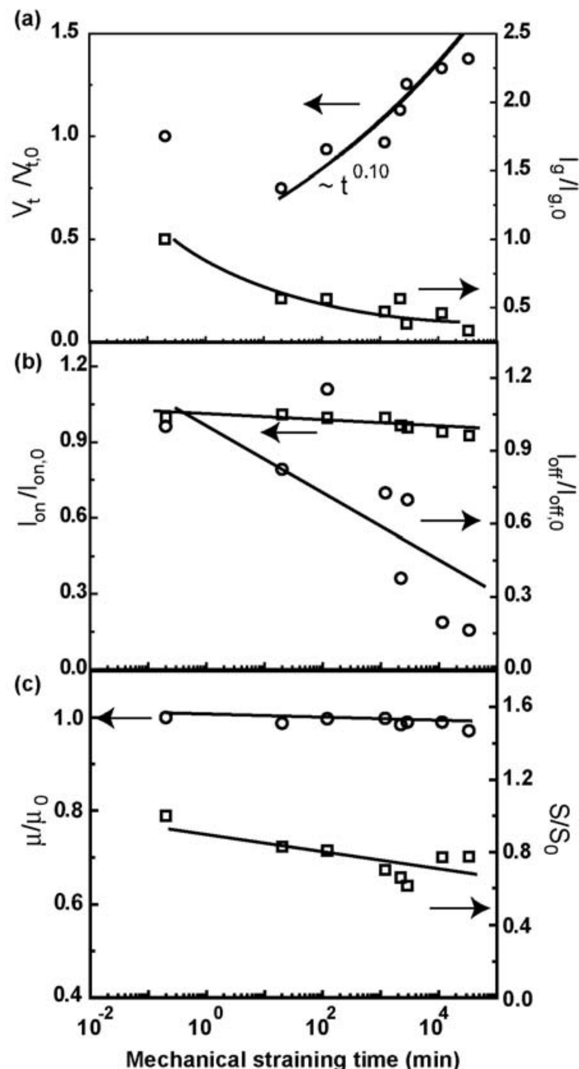

Fig. 2 . a-Si:H TFT performance after 1.8% mechanical compression for up to 33,000 minutes. (a) Normalized threshold voltage $V_t/V_{t,0}$ and gate leakage current $I_g/I_{g,0}$. (b) Normalized "on" current $I_{on}/I_{on,0}$ and "off" current $I_{off}/I_{off,0}$. (c) Normalized field effect mobility μ/μ_0 and subthreshold slope S/S_0. All data are normalized to the values for the as-fabricated TFT, entered at t = 0.2 minutes (subscript "0").

Electrical bias-stability at elevated temperatures

With the increase in temperature, the TFT transfer curves shift to the left and the gate leakage currents increase significantly. The exponential dependence of the gate leakage current on the gate voltage is caused by the tunneling or field emission inside the dielectric [9]. We extract the threshold voltage V_t at $I_{ds} = 10^{-8}$ A, the on current Ion at V_{gs}=25 V, and the off current at $V_{gs} = -5$ V from the transfer curves of $V_{ds} = 10$ V. Figure 3 shows the threshold voltage and on-off current ratio (I_{on}/I_{off}) against the substrate temperature. Raising the temperature from 20°C (293 K) to 55°C (328 K), the threshold voltage drops about 4 V, which is mainly caused by the thermal excitation of carriers. The on current increases from 10 to 40 μA while the off current increases more than one order of magnitude, which leads to the decrease in I_{on} / I_{off} at high temperatures. The I_{on} / I_{off} drops dramatically from 10^7 to 10^6 at ~50°C (323 K).

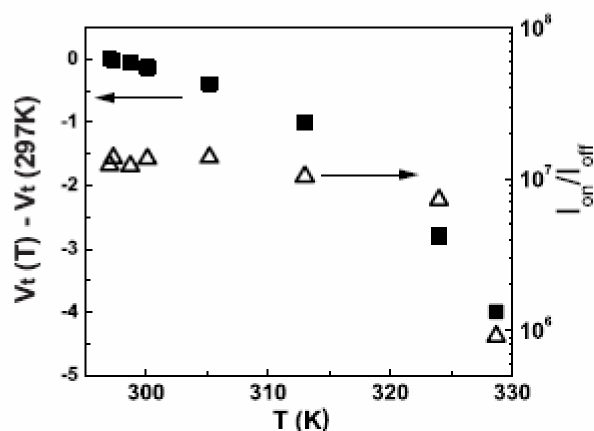

Fig. 3. Drop of threshold voltage and on-off current ratio vs. temperature.

The off current in the TFT arises from charge injection at the contacts, thermal generation in the channel, charge emission from the channel, and gate leakage current due to a nonideal gate dielectric. In our devices, charge injection from the contacts and charge emission from the channel are both negligible because the n+ source-drain contacts block the hole injection, and the TFT measurements were taken when temperatures reached steady state. Therefore, the off current in our devices mainly results from the thermal generation and the gate leakage current. The rise in off current for more negative V_{gs} indicates the conduction of hole current, with holes supplied from thermal excitation. Figure 4 shows that the gate leakage current increases with temperature. This temperature dependency of gate leakage current I_{gs} ~ 1/T is the evidence for Poole–Frenkel emission of trapped charges inside SiN_x gate dielectric. The dramatic increase in the gate leakage current also occurs at ~50°C (323 K), around the same temperature that the I_{on} / I_{off} suddenly drops. Therefore, the sudden increase in the off current above 323 K is mainly caused by the gate leakage current. The sudden rise in gate leakage current and off current at ~50°C (323 K) is also supported by the phenomenon observed in gate-bias stress experiments performed at elevated temperatures. Figure 5 shows the threshold voltage shift ΔV_t versus stressing time for TFTs under gate-bias stressing at different temperatures. Electrical gate-bias stressing causes very severe ΔV_t at high temperatures because of the faster defect creation rate inside the a-Si:H layers. Figure 5(a) clearly shows a saturation of ΔV_t beyond 50°C (323 K). The Arrhenius plot of ΔV_t after 1850s of gate-bias stressing is shown in Fig. 5(b). The activation energy dramatically drops and becomes constant for temperatures greater than 50°C (323 K). This saturation phenomenon beyond a certain temperature is different from the results reported in the literatures [4-7], where TFTs being studied were fabricated at temperatures of 300 °C or above.

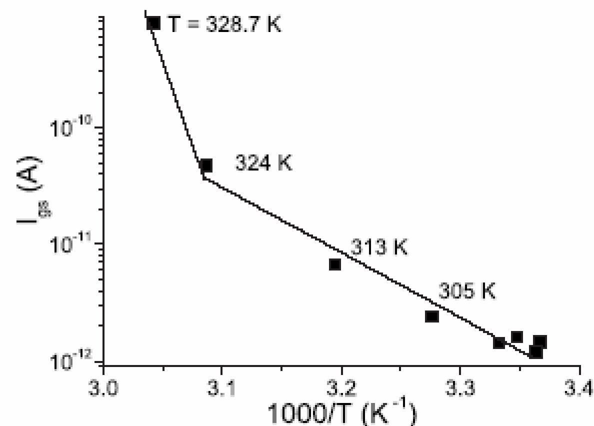

Fig. 4. Arrhenius plot of gate leakage current vs. temperature.

Based on the above observations, this study concludes that a large amount of charges, trapped inside the dielectric SiNx during TFT fabrication and gate-bias stressing, was thermionically emitted into the channel by the Poole–Frenkel mechanism at a temperature of 50°C (323 K). Since the charges trapped inside the gate dielectric cause ΔV_t, the

thermionic emission of the trapped charges leads to the saturation of ΔV_t. This phenomenon was observed in our low-temperature processed TFTs because the gate dielectric is less stable and the trapped charges are much easier to release at relatively low temperatures.

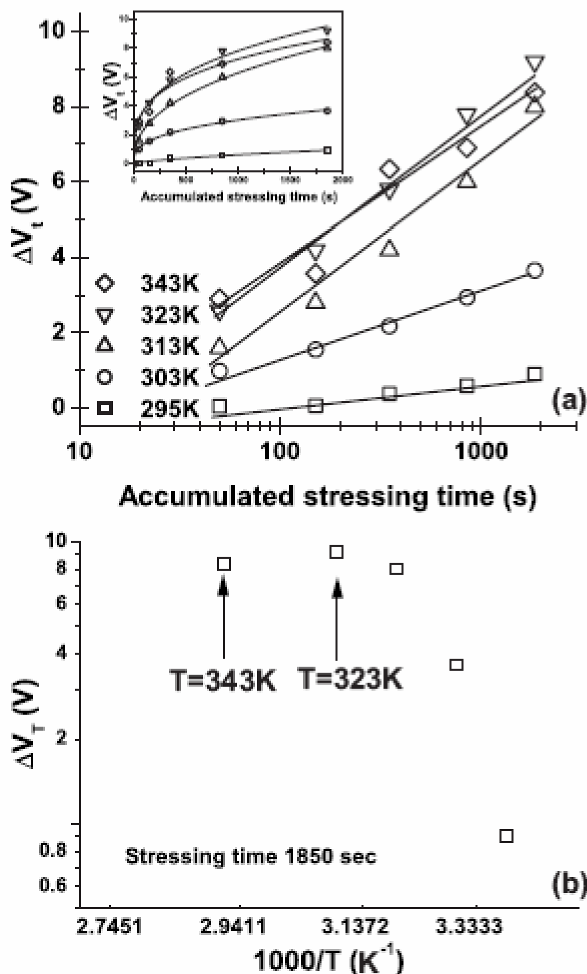

Fig. 5. (a) Shift of threshold voltage ΔV_t under electrical gate-bias stressing at various temperatures. (b) Arrhenius plot of ΔV_t after 1850s of gate-bias stressing.

4. Summary

We studied the effect of prolonged mechanical strain on the electrical characteristics of thin-film transistors of hydrogenated amorphous silicon made at a process temperature of 150ºC on 51-μm thick Kapton polyimide foil substrates. Effects are observed only at very high compressive strain of 1.8%. The TFTs were stressed for times up to 23 days by bending around a tube with axis perpendicular to the channel length, and were evaluated in the flattened state. The changes observed are small, which indicates mechanical stress short of values that cause fracture has little permanent effect on a-Si:H TFT performance.

In the study of electrical bias-stability at elevated temperatures, our low-temperature processed TFTs show an abnormal saturation of ΔV_t at 50°C (323 K) in a constant gate-bias stress experiment. Around the same temperature, we observed abrupt increases in both the gate leakage current and the off current. This abnormal saturation phenomenon is caused by the Poole–Frenkel emission of the charges, trapped inside the dielectric during TFT fabrication and gate-bias stressing.

5. Acknowledgements

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6. References

1. S. Wagner, H. Gleskova, J. C. Sturm, and Z. Suo, Technology and Applications of Hydrogenated Amorphous Silicon, R. A. Street, Ed. Berlin: Springer, p222 (2000).
2. H. Gleskova, S. Wagner, and Z. Suo, Mat. Res. Soc. Proc. Vol. **508**, p73 (1998).
3. H. Gleskova, S. Wagner, and Z. Suo, Appl. Phys. Lett. Vol. **75**, p3011 (1999).
4. M. J. Powell, Appl. Phys. Lett. Vol. 43, p597 (1983).
5. F. R. Libsch and J. Kanicki, Appl. Phys. Lett. Vol. **62**, p1286 (1993).
6. M. J. Powell, C. van Berkel, and J. R. Hughes, Appl. Phys. Lett. Vol. **54**, p1323 (1989).
7. W. B. Jackson, J. M. Marshall, and M. D. Moyer, Phys. Rev. B Vol. **39**, p1164 (1989).
8. H. Gleskova and S. Wagner, IEEE Trans. Electron Devices, Vol. **48**, p1667 (2001).
9. S. M. Sze, Physics of Semiconductor Devices, 2nd ed. Wiley, New York, (1983).