A Novel Design of Low Noise On-panel TFT Gate Driver

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Abstract

In this study, we redesigned the reliable integrated on-panel display gate driver that was equipped with dual pull-down as well as controlled discharge-path structure to reduce the high voltage stress effect and realized with TSMC 0.35 um CMOS-based technology before. An improved discharge path and a low noise design are proposed for our new a-Si TFT process implementation. Our novel reliable gate driver design can make each cell of shift register to be insensitive to the coupling noise of that stage.

1. Introduction

Amorphous silicon (α-Si) and poly-crystalline silicon (poly-Si) Thin-Film Transistors (TFTs) have been widespread used in mobile applications due to their low fabrication cost with simple process and high yield rate. However, more pixels means more interconnection lines required between the driving circuit and the pixel array. Accounting for the cost and complexities of packaging and assembling, the integrated On-Panel Drivers (OPDs) provides an effective solution. Therefore , much less external connections required between driver IC and display panel, to integrate the gate driver on a-Si TFT-LCD display panel seems to be the trend of modern consumer electronic products. It should be a good choice for high-solution display. Unfortunately, some TFTs in gate driver circuit, such as the output driving transistor and pull-down transistors, suffer high voltage stress for a long time that will cause their threshold voltage increasing and driving margin degradation[1]. In order to release the voltage stress of the pull-down transistors, the dual pull-down technique[2][3][5] doubling the number of pull-down transistors, has been proposed to share the turn-on cycle and to reduce the turn-on time of each transistor. Furthermore, an additional discharging path has been proposed to release the voltage stress of the output transistor [4]. However, the long-time floating state of the output node of each cell is a sensitive terminal which suffering seriously the noise coupling as a result of the periodic-clocking operation of that stage. An anti-fluctuating structure is proposed in [6].

In this paper, we discuss the above-mentioned topics of our modified reliable gate driver. The dual pull-down structure is the first topic, after that is the redesigned discharge path topic for the output transistor, and then is the third topic of low noise design for overcoming the floating problem. Finally, in order to reduce the space of our modified gate driver, we integrated the low noise design into the dual pull-down structure. Furthermore, we overcome the voltage stress and the floating problem at the same time. After simulation with the HSPICE level-40 for the a-Si TFT process model, it shows that our work has significant functional achievement and has much less noise than that of the conventional one.

2. A On-panel TFT Gate Driver with dual pull-down structure and discharge path

A gate driving unit for a selection line provides a high pulse voltage to each row line by turns. When gate driver turns on a row of TFT, source driver provides a voltage of data to charge pixels. After the pixels are charged, the gate driver provides a low voltage to keep the charge in the pixels and turns on next row line. Fig. 1 shows the block diagrams for gate drivers controlled by two-phase clocking (C1 and C2) comprising a series of shift registers to select row lines in scanning. Fig.2. is a gate driving unit for a selection line with dual pull-down path structure and discharge using CMOS-based technology [6] and has been realized before. In this structure, we use two pull-down transistor T3、T4 for node P1 and T5、T6 for output. Additionally, we add a discharge path to reduce the high voltage stress time for push-up

transistor (T2). We can observe the timing diagram of Fig.2 as show in Fig.3.

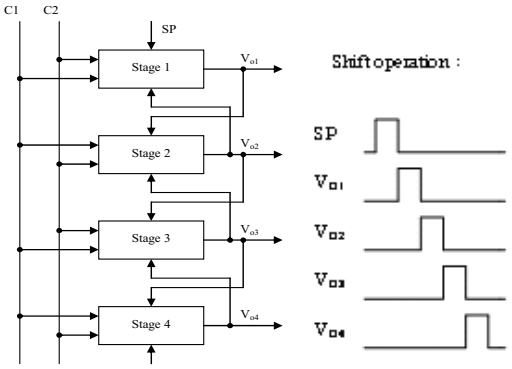

Fig. 1. The block diagram of Gate Driver and its shift operation for gate scanning.

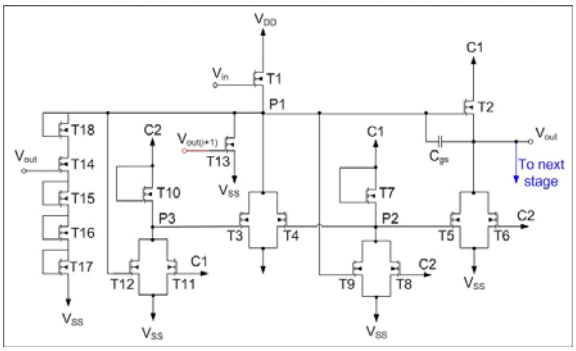

Fig. 2. A gate driver with dual pull-down structure and discharge path using CMOS-based te chnology [6].

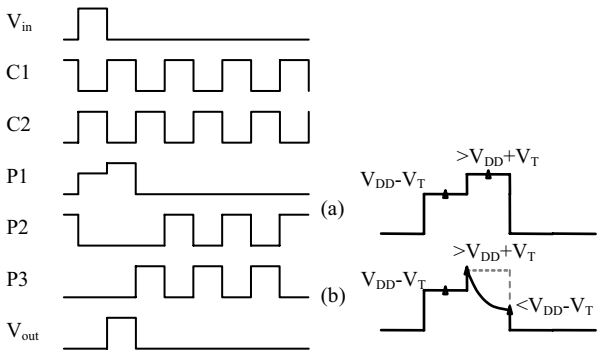

Fig. 3. The timing diagram of Fig.2 and the voltage waveform of node P1.

The dual pull-down transistor pairs turn on alternately until V_{in} provide a high voltage and they will be turn on sequence. The boosting technique would cause charge injection in the parasitic gate capacitance, C_{gs}, to promote the gate voltage in the conducting period. In such way, the main problem encountered when the push-up transistor (T2) would suffer serious stress effect. The reason is that charge injection would produce the high voltage stress. For this reason, we add a discharge path to reduce the high voltage stress time for push-up transistor. Thus, the node P1 will be discharged by discharge-path to release the high gate stress of driving TFT. Some additional TFTs are needed to control the dual pull-down transistor and discharge path.

In this paper, all of the design was used α-Si TFT-based technology. Due to the lower mobility of TFT used, we modified the dual discharge-path as shown in Fig.4 to reduce the higher voltage stress time for push-up TFT (T2). In the first discharging duration, one of discharge-path TFT (TD1) will be turn on gradually and be used to discharge node P1 which output voltage rising. When output voltage has risen to its full high level, another discharge-path TFTs (TD2&TD3) will also turn on and be used to discharge node P1. In the second discharging duration, all of the discharge-path TFTs will turn on completely and we can see dual discharging as shown in Fig.5(b).

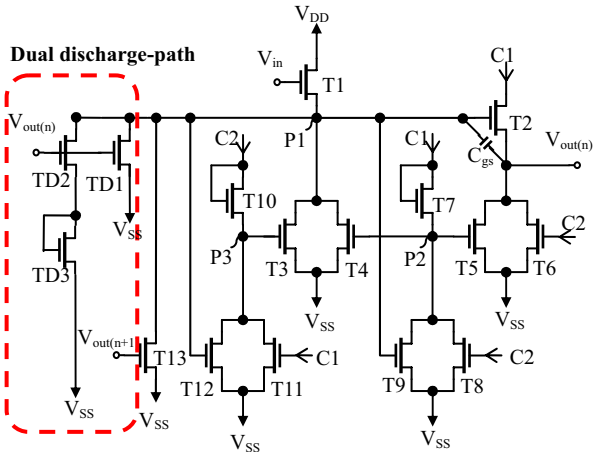

Fig. 4. A gate driver with dual pull-down structure and modified discharge path using α-Si TFT-based technology .

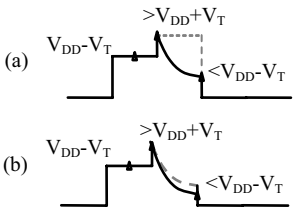

Fig. 5. Voltage waveform of node P1 (a) with a discharging path; and (b) with a dual discharging path.

The node P1 voltage can't be allowed discharge too fast. Otherwise, the voltages of nodes P2 and P3 are not at low level to make transistors T4 and T5 turn off. It was also found that the too small voltage at the node P1 should fail to keep the charge of the pixel of the

LCD cells. Therefore, we must design the discharge path with a suitable size of TFT remains a proper voltage after discharged. The discharge speed is given by the following equation (1):

$$I = \frac{Q}{\Delta t} = \frac{C \cdot \Delta V}{\Delta t} \qquad (1)$$

3. A Novel Design of Low Noise On-panel TFT Gate Driver

In order to achieve the enough driving capability, the size of push-up TFT (T2) must be larger than that of others. As a result, the coupling effect is happened easily on the larger parasitical capacitance of push-up TFT. Such fluctuation noise is resulted from the charge injection by means of the coupling of clock C1 to the node P1 by C_{gd}, and then to the output by C_{gs}. Therefore, the node P1 is located at the key point on the fluctuating influence path. For this reason, the output voltage is fluctuating seriously while no output pulse is shifted.

In this paper, we proposed a modified on-panel TFT gate driver with anti-fluctuating structure in conjunction with the stress-reducing effect as shown in Fig.6 to reduce the noise coupling from C1 [6]. Moreover, to decrease the number of TFTs, the anti-fluctuating structure is integrated into the on-panel TFT gate driver with dual pull-down structure and discharge path. Here, a modified discharge-path (T8) to reduce the duration of the required higher boosted voltage of node P1 for driving the output pull-up TFT (T2) is redesigned. In order to keep the output node $V_{out(n)}$ from the ac coupling of clock C1, the voltage of node-P1 must keep low enough constantly, an anti-fluctuation structure (T9-T11) is added and a low stress voltage node P3 is designed for the pull-down TFT(T9) of node P1. The voltage of node P3 is reset to V_{SS} each time when the input pulse V_{in} is coming in order to not affect the proper bootstrapping-up operation of node P1. But at some time late, while the output pulse $V_{out(n+1)}$ of the next stage is fed back , the node P3 will be biased and held at an appropriate small voltage level which is still large enough to pull down the node P1 voltage through T9 by optimized-design of the size of T10 and T12. This situation is sustained until the coming of input pulse V_{in} of the next scan-turn. The connection of node P1 to a small constant voltage by a low resistance path as described above keeps it from the coupling of clock source C1 efficiently. An improved low-noise structure consists of a modified discharge path, a dual pull-down and an anti-fluctuation portion. The novel design of low noise on-panel TFT gate driver would be not only reduced the fluctuating noise of output but also improved the serious stress effect.

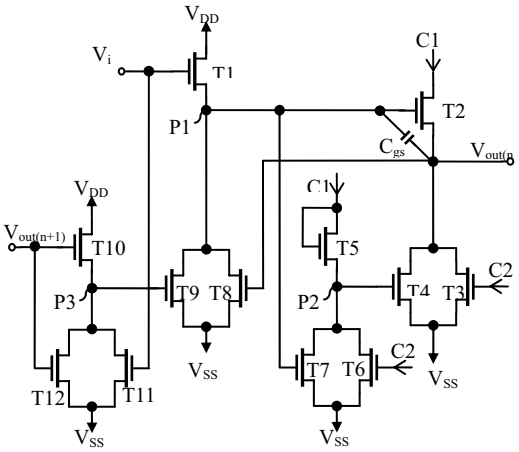

Fig. 6. A novel design of low noise on-panel TFT gate driver.

4. Simulation results and discussion

In this paper, simulation with the level=40 of α-Si TFT process Spice Model and the operation voltage is used from +10V to -10V. Fig.7 and Fig.8 illustrate the waveforms of the voltages at the clock P1, the input, the node P1 and the output in the circuits shown in Fig.2 CMOS-version and Fig.4 TFT-version respectively. The node P1 voltage would be boosted by clock C1 from low to high. Therefore, the higher voltage is stressing on push-up TFT (T2). After that, the node P1 voltage drops to low voltage due to the turn-on of discharge path. Additional TFTs can reduce stress time of push-up TFT effectively.

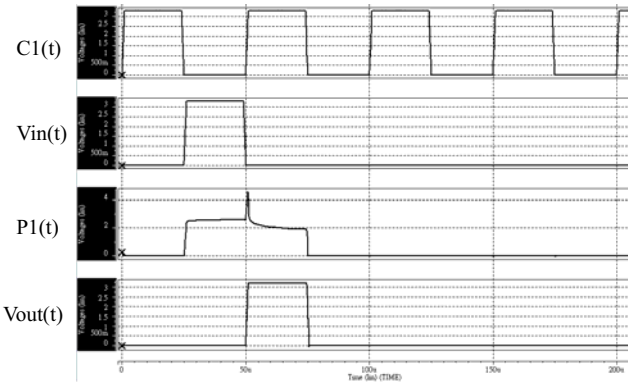

Fig. 7. The simulation results of the circuit as show in Fig.2 that using TSMC 0.35UM Mixed Signal 2P4M Polycide 3.3V Spice Model [6].

Additionally, referring to simulation results as shown in Fig.8, the fluctuation problem occurred on the output pulse due to the parasitic capacitance

coupling from the transition of clock C1. Fig.9 illustrates the waveforms of the voltages at the output Vout(n), the node P1 and the node P3 of our proposed a novel design of low noise on-panel TFT gate driver with new anti-fluctuation circuit shown in Fig.6 by using the level= 40 of a-Si TFT process Spice Model with channel widths and lengths of TFTs designed from W/L = 20/5um to W/L = 2,000/5um, and the operation frequency is 20 KHz.

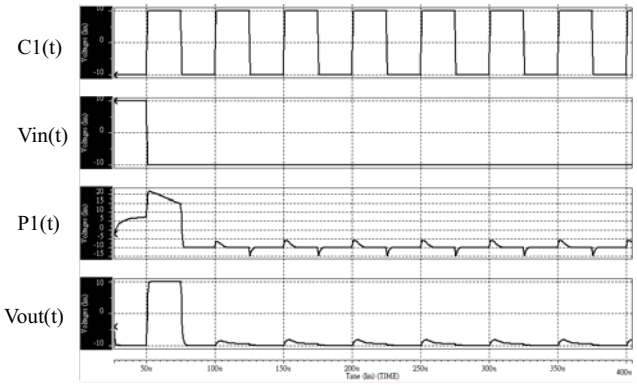

Fig. 8. The simulation results of the circuit as show in Fig.4 that using the level=40 of a-Si TFT process Spice Model.

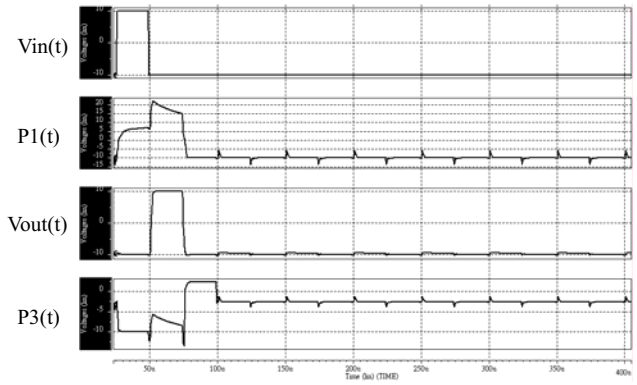

Fig. 9. The simulation results of the circuit with low noise as show in Fig.6 that using the level=40 of a-Si TFT process Spice Model.

Here we can see, the voltage of node P3 is resets to the low voltage V_{SS} (-10V) first by the input pulse V_{in} at the beginning of each scan-turn, and then makes the pull-up TFT (T2) off at this time. After the completeness of output scan-pulse of this stage $V_{out(n)}$, and when the output scan-pulse $V_{out(n+1)}$ of the next stage is fed back late, the node P3 voltage will be set and held at a small voltage level (about -3 V) but large enough to turn on the T9 (V_{GST9} = 7V) , then the voltage of node P1 is pulled down to V_{SS} by T9 constantly until the start of this stage at the next scan turn. It is obviously, as comparing with Fig. 8 without anti-fluctuation processing, we overcome the fluctuation noise phenomena at the output voltage $V_{out(n)}$ successively by our proposed a novel design of low noise on-panel TFT gate driver.

5. Summary

In this study, we propose a novel total stress-reducing solution for the on-panel α-Si TFT-based gate driver of LCD display. In addition to use the dual pull-down and a modified discharge path structures to relax the stress effect of the output stage, an improved low-stress, anti-floating low noise structure is designed. According to the results of our simulation with the HSPICE level-40 for the α-Si TFT process model, it shows that our proposed structure works successively as expected to suppress the fluctuation n oise phenomenon at the output node and to relax the high stress of the related key-transistors. Thus it is a reasonable conclusion that the proposed structures in this paper for an on-panel TFT gate diver can operate well with good reliability and low noise

6. References

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