Increase the reliability of the gate driver for amorphous TFT displays

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Abstract

In this study, we used a multiple phase scheme for the clock in the dual-pull-down driver for TFT display panels. In this scheme, the turn-on time for the transistors in the dual-pull-down structure was reduced from 1/2 to 1/4 or 1/8 of the period cycle time. While keeping proper operation of the transistor size of circuit was fine tuned to achieve an optimal performance. The relation between the active time and the transistor dimensions was obtained for the optimal design.

1. Introduction

As TFT device in a long time in the on-state, will cause IV curves of drift, we call the phenomenon, which is stress effect. This phenomenon would let the threshold voltage leading to increased. That's effect making the current driving force of TFT smaller, when the threshold voltage increases to a certain value, the supply voltage can't even drive TFT.

Figure 1(a) is the block diagram of traditional TFT gate driver circuit. The gate drive circuit by the circuit string of multi-level access from [1]. These control signals of gate driver circuit C1, C2 and the start signal SP initiate the operation of as shown in Figure 1(b). Figure 2 shows a traditional TFT gate driver circuit, which consists of six transistors and a capacitor and work timing diagram. Table I shows the turn-on time of the traditional TFT gate driver circuits for use in the resolution of QVGA. The status of it is under serious stress effect, the threshold voltage of T2 and T6 increases to lower TFT gate drive circuit capability, and makes circuits in the P1 and Vout node voltage not through transistor T2 and T6 maintained at a low potential, making the functions of circuit failure. In this structure of the circuit, the first should focus on improving the serious stress effect part of the circuit can maintain a normal work longer.

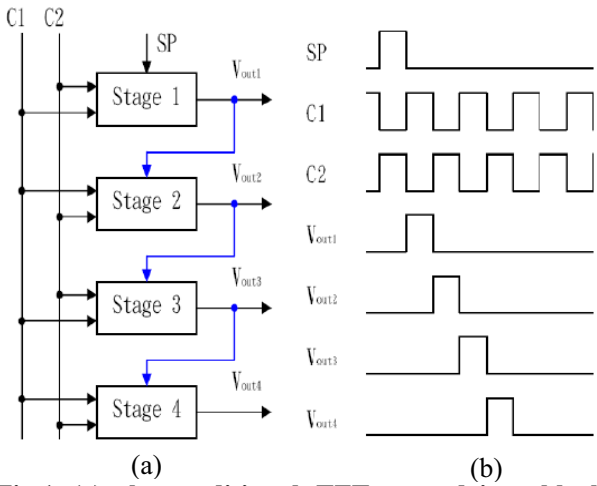

Fig.1 (a) the traditional TFT gate driver block diagram (b) shift operation for gate scanning

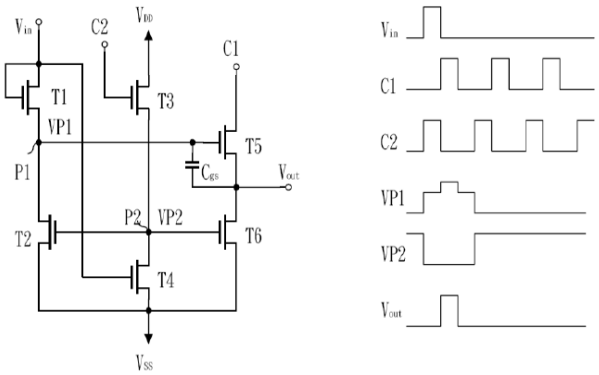

Fig.2 Circuit of the traditional TFT gate driver and work timing diagrams.

Table I Traditional TFT gate driver circuits for use in the resolution of QVGA.

QVGA(240*RGB*320)	Turn-on ratio (Duty Cycle)
T1 、 T4	1/320 ≈ 0.3%
T2 、 T6	317/320 ≈ 99.06%
T3	1/3 ≈ 33.33%
T5	3/320 ≈ 0.94%

2. Experimental

Dual pull-down Structure main objective is to make use of this structure will to replace the original traditional TFT gate driver circuit stress effect in the most serious single pull-down TFTs. We'll make the overall circuit of the key, which is the TFT to reduce the working time so as to reduce the Stress Effect. In order to the increase the gate driver working time, let circuits maintain its original function and add the Pull-down transistor. In this way, control circuits make use of control signals are part of the overall transistor circuits and control signals pose[2][3][4][5][6].

We used the dual-Pull-down structure, which's on-time ratio reduced to 1/2. Table I is able to tell us T2 and T6 are almost working, so we have been introduced to a modified Figure 3 dual pull-down structure TFT gate driver circuit block diagram of this study to increase by the transistor of lifetime, thereby enhancing TFT-LCD panel reliability. In addition, we use of four-phase clocking to reduce the turn-on time of the pull-down transistors. These first, the lifetime of the TFT circuit would be enhanced significantly.

In this project would promote the feasibility of the TFT gate driver on the display panel. We based on the use of two non-overlapping clock (C1, C2) and (C3, C4), of which, (C3, C4) but do not overlap with (C1, C2) synchronization, for the duration of (C1, C2) of the relative time 1/4 cycle.

As mentioned above, we added C3, C4 to replace the C1, C2 on transistors T7 and T10, as shown in figure5. The duty cycle of C3, C4 was reduced down to 1/4. The use of 4-phase clocking will reduce the conduction time of the pull-down transistors. Therefore, the lifetime of the gate driver would be enhanced significantly.

In this design, a quadruple-phase clock scheme with reduced duty cycle time was applied to activate the operation of the pull-down networks while keeping the circuit functioning correctly.

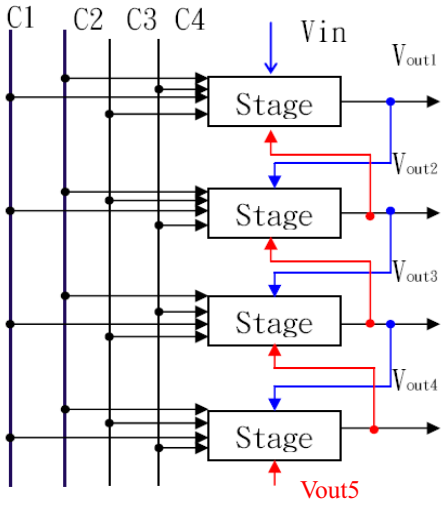

Fig.3 Modified Dual-pull down TFT gate driver circuit block diagram

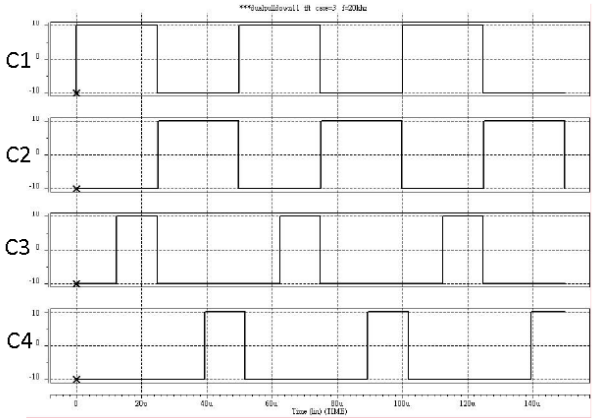

Fig.4 Input dual-pull-down at the clock signal.

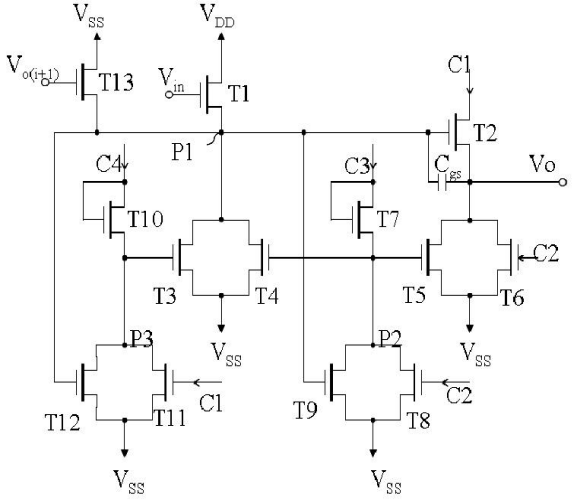

Fig.5 Dual pull-down gate driver circuit.

3. Results and discussion

This study would increase the reliability of the on panel TFT gate driver circuit. With the above signal source, we used the α-Si TFT model. From the figure 6, we will dual pull-down for the original signal source by 1/4 after both dual-pull-down of P2 and P3 nodes can be observed that the transistor on-time into the original 1/4, which can effectively reduce the impact of stress effect, and can achieve high gate driver circuit reliability.

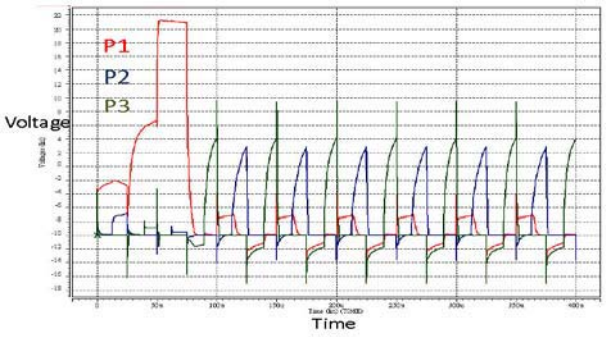

Fig.6 For a-Si TFT gate driver circuit of the w aveform.

We put forward this idea for the original signal source by 1/4. Figure 7 shows the signal waveforms is one stage. In that figure shown which reduce the source signal also to have possession of the normal working-wave output.

Similarly know about we try to simulate multi-level output. However, we find that after a multi-level circuit. That was obviously not sufficient to promote the ability to drive the third grade output. Therefore, we change this circuit transistor size, for the purpose of to increase circuit drive capability also shown in figure 8.

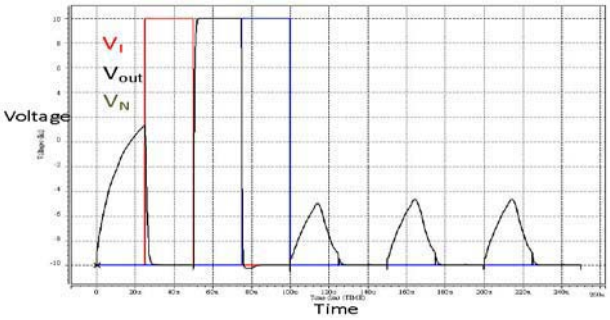

Fig.7 Output waveform of one stage.

This way, we will try to simulate more level of output waveform. We're to observe the increase in size after the transistors, can work in normal multi-level circuit in figure 9.

From the figure we can see as the result of the multi-level output still has reached a stable work voltage. The original signal source by 1/4 was adopted, wherefores which was better than the original signal source by 1/8. However, the original signal source by 1/8, although the transistor on-time ratio lesser than 1/4.

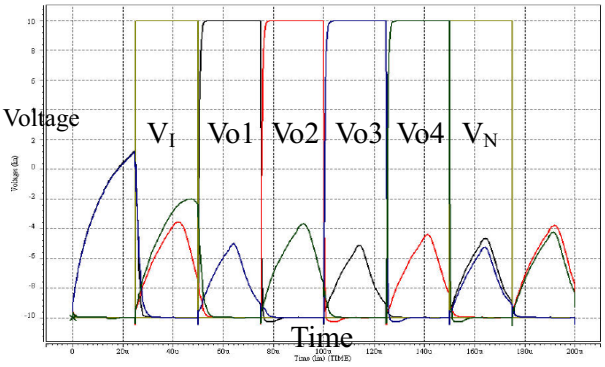

Fig.8 Four stage output waveform.

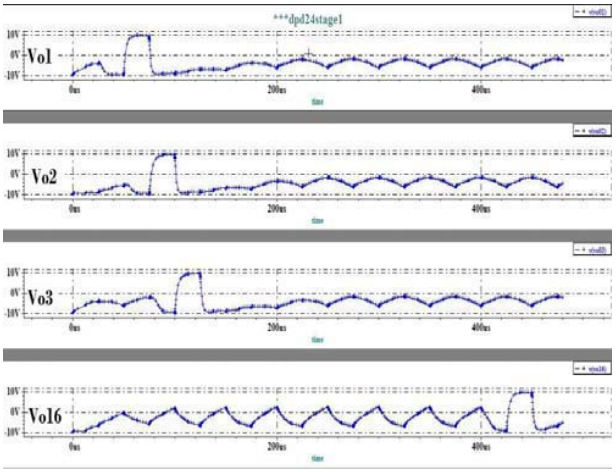

Fig.9 Multi-level stage output waveform.

But the original signal source reduce eighth will allow transistors to increase the size of the original four times the size or more as shown in Table III. That was after multi-level circuit to normal work. We can clearly see from Table II when the transistor on-time ratio.

Table II Modification clock TFT gate driver circuits for use in the resolution of QVGA TFT when all the on-time Ratio.

QVGA(240*RGB*320)	Turn-on ratio (Duty Cycle)
T1	1/320 ≈ 0.3%
T2、T9、T12	2/320 ≈ 0.6%
T3、T4、T5、T7、T10	80/320 ≈ 25%
T6、T8、T11	160/320 ≈50%

Table III Modification clock TFT gate driver circuits on-time Ratio.

QVGA Size	Turn-on ratio (Duty Cycle)		
	50%	25%	12.5%
T7	20x5 μ m2	40x5 μ m2	180x5 μ m2
T10	20x5 μ m2	40x5 μ m2	180x5 μ m2

Finally, for the integration of this study is the reduction of floating effect by the latest TFT gate drive design as show figure 10. The analysis showed that the output voltage fluctuations due to the phenomenon of C1 is driven by exports of TFT (T2) of the T2 Cgd coupled to the gate P1, again by Cgs coupled to the output point Vout(n), this floating P1 coupled effect of the key points. The purpose of this design by using the drop-down TFT (T9) most of the time to pull P1 voltage to low voltage VSS, by this way for the eradication of the design, control circuit composed by the three transistor (T10, T11 and T12). Current level output signal Vout (n +1) have, immediately started floating effect of the reduction circuit, T10 and T12 on-P3 will be maintained at an adequate on-T9 low voltage, P1 voltage through the T9 to VSS, capacitance coupling effect could reduce.

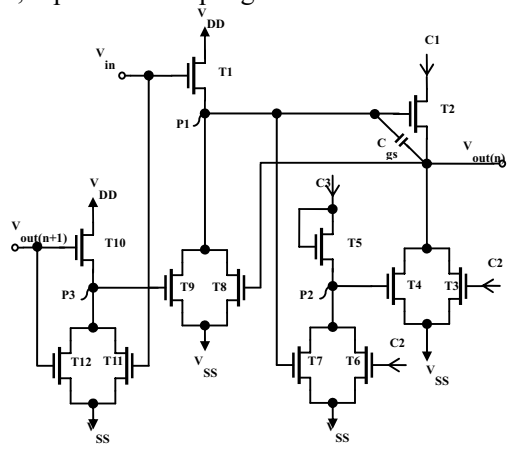

Fig.10 anti-floating TFT gate driver

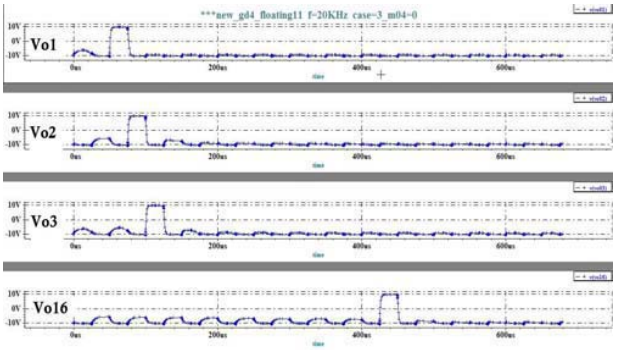

Fig.11 Anti-floating TFT gate driver output waveform.

4. Summary

Table II for the modification clock TFT gate driver circuits for use in the resolution of QVGA TFT when all the on-time ratio of (Turn-on ratio). Table II details of the T2 and T6 almost to lie on the on-state. We can observe from Table II, that T3、T4、T5 the on-time ratio of (Turn-on ratio) reduced to the original circuit of 1/4.

The circuit through the use of LEVEL = 40 of the α-Si TFT process Spice model simulation results showed that, indeed success achieve reduce transistors on-time ratio. After adjusting the size of transistors, circuits can achieve the stability of multi-level output.

5. Acknowledgments

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6. References

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