Three Dimensional Architecture of Multiplexing Data Registration Integrated Circuit for Flat Panel Display

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Abstract

As Flat Panel Display become large in format, the data and gate lines turn into longer, parasitic capacitance and resistance increase, and the display signal is delayed. Three dimensional architecture of multiplexing data registration integrated circuit method is used that divides the data line into several blocks and provides the advantages of high accuracy, rapid selection, and reasonable switching speed.

1. Introduction

The design concept can be easily scaled up for large array format TFT-LCD elements system without much change in the terminal numbers thanks to the three dimensional hierarchy of control circuit design, which effectively reduces the terminal numbers into the cubic root of the total control unit numbers and prevent a block defect of the flat panel[1-3]. The TFT-LCD unit lights, line(s) in the vertical or horizontal axis appear dim[4-5], but not completely on or off. These defects are generally the result of a failure in the row (horizontal) or column (vertical) drivers or their connections. The TFT-LCD includes an extension part defect such as an extension piece overlapping with a pixel electrode of boundary pixels at a boundary data line applying a data signal to the boundary pixels.

2. Experimental

A flat panel display with three dimensional architecture of multiplexing data registration integrated circuit having a plurality of scanning electrodes, a plurality of data electrodes extending perpendicularly to the scanning electrodes, and liquid crystal filling a space between the scanning electrodes and data electrodes, pixels being formed at each intersection of the scanning and data electrodes together with the liquid crystal, the display panel being divided into an even row part and a odd row part; a scanning control circuit for scanning the scanning electrodes by sequentially supplying scanning voltages to each scanning electrode and by maintaining the same for a predetermined period, the scanning electrodes located in the even row part of the panel and the scanning electrodes located in the odd row part being scanned separately but simultaneously in the same directions from upper to lower of the panel; an image data control circuit for sequentially supplying image data voltages to the data electrodes in synchronism with scanning of the scanning electrodes, the scanning electrodes are scanned in such a manner that the image data is written on the pixels in a selecting period, the written image data is held on the pixels in a holding period and the image data is eliminated in an eliminating period;

3. Results and discussion

In traditional control circuit design for TFT-LCD elements array system, each TFT-LCD element requires one driver switch. As a result, when the TFT-LCD pixels scale up into a large array, the numbers of input/output ports will increase enormously. To handle large array of driving circuits for such large pixels array, 2D circuit architecture was employed for the traditional driving circuit to reduce the IO number from n*n into 2n+1. However, firstly, this reduction still can not meet the requirement for high speed

signal scanning with low data accessing points when switch numbers greater than 640×480 pixels. It would be necessary to increase the display frequency to 240 Hz or higher to eliminate flicker. If the display frequency is 240 Hz, a period of time for writing one frame is 4.17 ms. Assuming the number of scanning electrodes is 480, a period of time available for writing one line is only 8.7 microseconds. The number of scanning electrodes has to be larger than 480 to display a high resolution image, making the writing period further shorter. Secondly, no technology is ever completely perfect, of course, and the LCD can still suffer from some defects in the displayed image. In this technology, though, most defects in the basic electronics, such as failure of the backlight or the row or column drivers, result in a completely unusable display, and so when such occur in production they are easily detected and corrected. It is extremely rare for a product to ship with any such problems.

To achieve this, In this study, a three dimensional data registration flat panel display scheme(Fig. 1) to reduce the number of data accessing points as well as scanning lines for large array TFT-LCD element with switch number more than 640×480 is proposed(Fig.2). The total numbers of data accessing points will be $N=3\times\sqrt[3]{Y}+1$, which is 68 for 640×480 switches by the 3D novel design, the scanning time is reduced up to 30% (The scanning speed is also increased by 3 times) thanks to the great reduction of lines for 3D scanning, instead of 2D scanning.

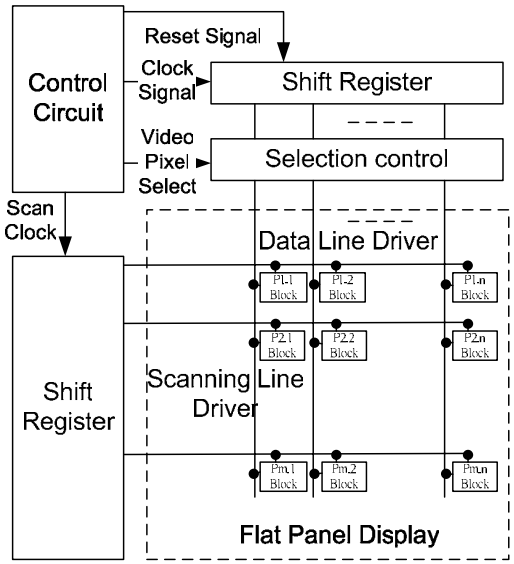

Fig. 1. Three dimensional data registration flat panel display

The display panel is divided into many scanning block part, both parts are separately and simultaneously scanned in the same directions to write images on the pixels on the respective scanning electrodes. This scanning is called multi scanning. For example, the lower part is scanned from the center of the panel toward the lower edge of the panel, while the upper part is scanned from the center of the panel toward the upper edge of the panel in synchronism with the scanning of the lower panel. The upper block image is displayed in the first field in which all the scanning electrodes in both parts are scanned, and the lower part image is displayed in the second field following the first field. The first and second fields constitute one frame of the displayed image. The image is written on the pixels in a selecting period, held in a holding period and eliminated in an eliminating period. Many selection data block and scanning block provide the advantages of high accuracy, rapid selection, and reasonable switching speed.

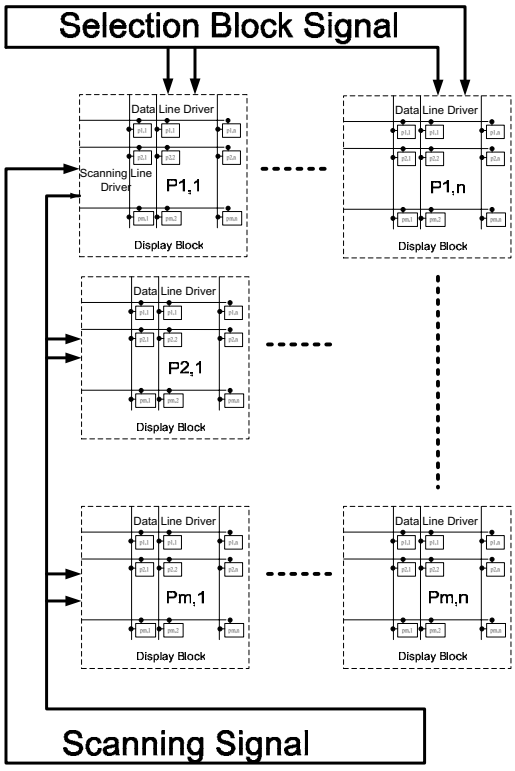

Fig. 2. 3D scanning display block array

The comparison among 1D, 2D, and 3D architectures is listed in Table 1. As the number of pixels increases, a driving circuit with higher dimension can effectively reduce the connections. To illustrate the effectiveness of the circuit dimensional to accommodate pixel elements, three curves for calculating the pad connections from 1D, 2D, and 3D control circuits are shown in Fig. 4. The 1D case increases most rapidly while the 3D one increases slowest. There are two important intersections among the three curves, with the first one in a nozzle number of 10 and the second one in 30, which means 1D circuit suitable for controlling less than 10 pixel elements while 2D circuit better for tens of pixel elements. When the number of pixel elements is increased significantly larger than 30, which may be in a range of hundreds to even thousands, a 3D architecture are necessary to reduce the number of pad connections into tens.

TABLE 1. Comparison among 1D, 2D, and 3D architectures

X:Pad connections、Y: pixel elements	***X~Y+1***		**(X : Connection lines ,Y : : pixel elements)**
Switches	1000	1024	1000
TFT LCD elements	1000	1024	1000
Interconnect Pad	1001	65	31
Scanning time	>90usec	90usec	30usec

The display panel being divided into an even row part and a odd row part; a scanning control circuit for scanning the scanning electrodes by sequentially supplying scanning voltages to each scanning electrode and by maintaining the same for a predetermined period, the scanning electrodes located in the even row part of the panel and the scanning electrodes located in the odd row part being scanned separately but simultaneously in the same directions from upper to lower of the panel;

In the Logic Analysis, the relationship between the ASIC input and output is shown in Fig. 3. The input signals include "DATA、CLK1、CLK2、CTRL、SETB" and the output signal match the designed ASIC signals very well.

Due to selection control signal, most defects in the basic electronics, such as failure of the backlight or the row or column drivers, result in a completely unusable display, and so when such occur in production they are easily detected and corrected. The image is written on the pixels in a selecting period, held in a holding period and eliminated in an eliminating period.

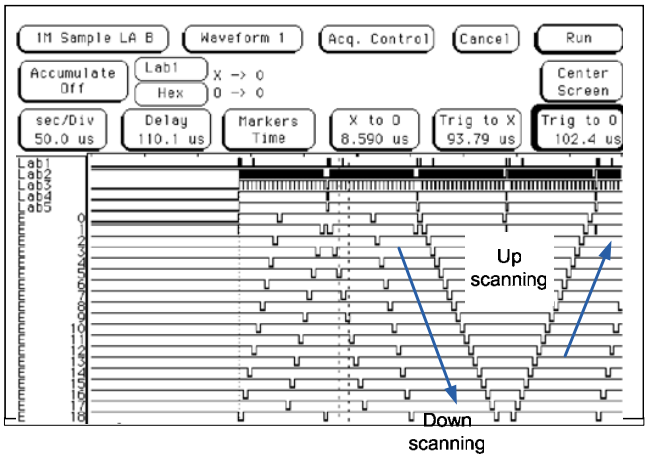

Fig. 3. The Logic Analysis signal of scanning block

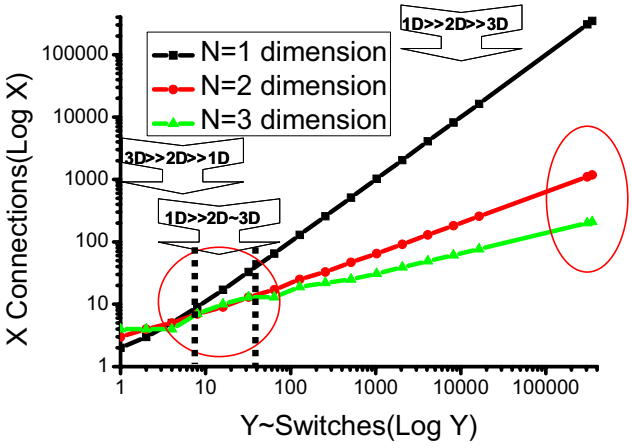

Fig. 4. Pad connections from 1D, 2D, and 3D control circuits

4. Summary

The design of the three dimensional hierarchy with control circuit, which effectively reduces the terminal numbers into the cubic root of the total control unit numbers and prevent a block defect of the flat panel. The display panel is divided into many scanning block parts, each part is separately and simultaneously scanned in the same directions to write images on the pixels on the respective scanning electrodes. These defects are generally the result of a failure in the row (horizontal) or column (vertical) drivers or their connections. We have reached the advantages of high accuracy, rapid selection, and reasonable switching speed flat panel.

5. References

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