Research of the TFT-LCD Photosensitive Resist Thickness

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We find some array mura are caused by S/D bridge or channel open in 4 mask process. The gray tone PR thickness non-uniformity is the main reason of these defects. By the adjustment of exposure and dry etch parameters, S/D bridge and channel open ratio drops by 10.87%.

1. Introduction:

4 mask process is the main technique used in the TFT-LCD (Thin Film Transistor-Liquid Crystal Display) manufacturing process. Fig.1 shows the 4 mask multiple etching process. It incorporates active mask and S/D (source and drain) mask process together. By the use of gray tone technique, channel pattern is produced with one exposure process. The PR (photosensitive resist) thickness and uniformity control are the crucial factor which will greatly influence the exposure result. The various kinds of defects such as PR remain and over etch are produced in the following etching process [1]. In this paper, we discuss how to control the uniformity of the PR thickness and eliminate the array mura caused by S/D bridge and channel open defects.

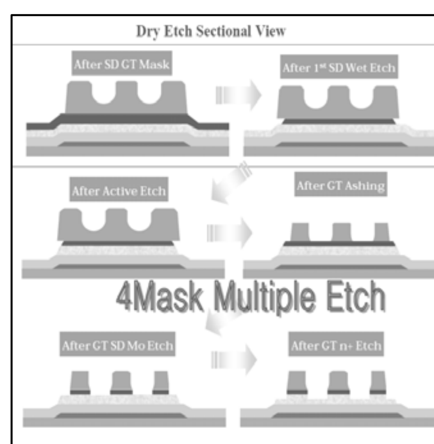


Fig.1 4 Mask Multiple Etch Process. 4 mask technology combines active mask and S/D (source and drain) mask process together.

2. Defect Mechanism Analysis:

A、S/D Bridge

The S/D bridge means the channel becomes narrower than the normal one at the whole TFT channel as shown in Fig.2. Mass bright array mura can be seen macroscopically. The array mura mainly occurs at the TFT panel edge statistically as shown in Fig.3.

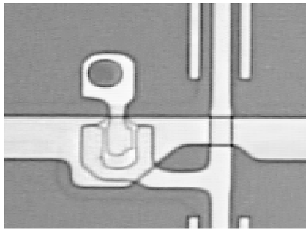


Fig.2 S/D Bridge Image. S/D bridge means the drain electrode becomes wide at the TFT channel.

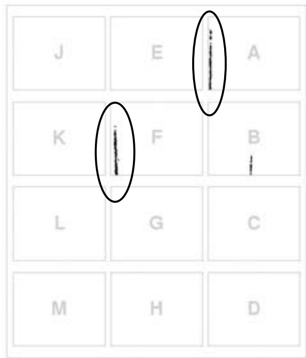


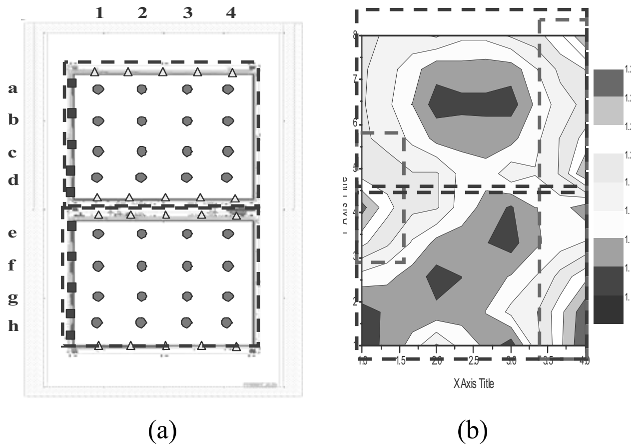
Fig.3 S/D Bridge Defect Position Map. By the statistic result, the array mura mainly occurs at the panel edge.

After PR coating process, PR thickness at the glass edge is higher than that in the center area as shown in Fig.4. In the following ashing process, PR at the glass edge could not be striped and remained. TFT channel pattern in that area becomes abnormal, and its W/L is relatively large.

Regarding to the switch off current calculation (I_{off}) formula:

$$I_{off} = q\sqrt{k/r}T^{3/2}e^{-Eopt/(2kT)}(\mu_c + \mu_p)V_D dW/L$$

In which W/L is the channel width/length; μ_c、μ_p is the field mobility of electrons and ions. V_d is the voltage between source and drain electrode; d is the thickness of a-si; k/r is the relative parameter of a-SiNx/a-Si interface. With the I_{off} increasing, pixel turns out to be in the undersaturated condition electrically. The charge quantity in the Cst (storage capacitance) decreases so drastically that pixel becomes a bright point.



(a) (b)

Fig.4 SDT Mask Measurement Pattern & Real Data Map. After PR coating process, PR thickness at the edge is higher than that in the center area. (a) is the mask measurement pattern. (b) is the real data map. The box areas at the edge are the S/D bridge defect area.

B、*Channel Open*

The channel open means the damage in a-Si layer on the TFT channel area as shown in Fig.5. The main mechanisms of channel open are: 1. PR thickness on the TFT channel area is too thin; 2. S/D layer is damaged to some extent after PR removal; 3. a-Si in the channel area is partially or totally overetched [2]. Fig.6 shows the 4 mask multiple etch SEM (Scanning Electron Microscope) image. The Formula of open current I_{on}:

$$I_{on} = -[(V_G - V_T)V_D - V^2{}_D/2]C_i\mu_{fc}W/L$$

In which W/L is the channel width/length; C_i is the capacitance per unit area; μ_{fc} is the field ion mobility; V_G、V_D and V_T are the gate voltage, source/drain and

threshold voltage. The carrier mobility drops down with the decrease of a-Si layer thickness. The switch on current I_{on} decreases too. Pixel area charges abnormally. The liquid crystal rotation becomes abnormal to lead to bright point.

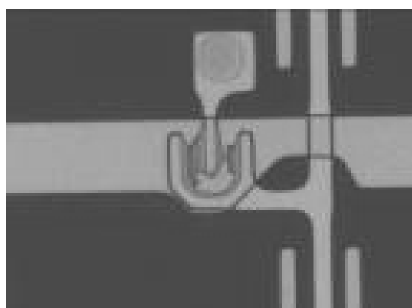


Fig.5 Channel Open Image. The Channel open means the damage in a-Si layer on the TFT channel area.

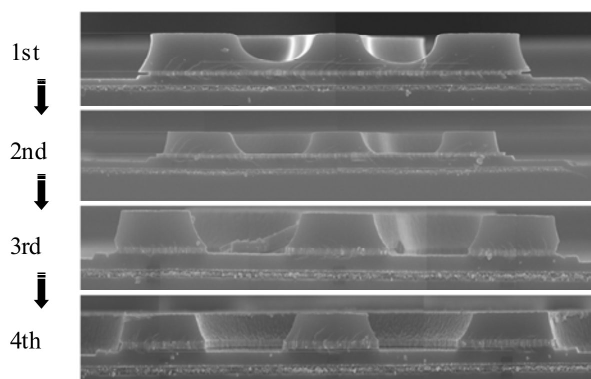


Fig.6 4 Mask Multiple Etch SEM Image (From Active Etch to n+ Etch). 1st is active etching; 2nd is gray tone PR ashing; 3rd is gray tone S/D Mo etching; 4th is gray tone n+ etching.

3. Method and Effect:

The S/D bridge and channel open are two interactional defects. The S/D bridge is inclined to occur with the relatively thick PR area or shorter etching time [3]. The channel open is inclined to occur with the relatively thin PR area or longer etching time condition [4]. After gray tone mask process, 600Å PR thickness increase is achieved around the channel area with the adjustment of exposure parameters. It minimizes the occurrence ratio of channel open. By increasing 7 seconds of ashing time in dry etching process, S/D bridge ratio is reduced effectively.

4. Conclusion:

The adjustment of gray tone mask and ashing process is demonstrated that the channel open and S/D bridge occurrence ratio decrease effectively. The ratio of Array Mura caused by S/D Bridge and channel open decreases from 11.25% to 0.42%. The production ratio is increased greatly.

5. Reference:

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