High mobility indium free amorphous oxide based thin film transistors

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(2 line spacing)

Abstract

High mobility bottom gate thin film transistors (TFTs) with an amorphous gallium tin zinc oxide (a-GSZO) channel layer have been produced by rf magnetron cosputtering using a gallium zinc oxide (GZO) and tin (Sn) targets. The effect of the post annealing temperatures (200 °C, 250 °C and 300 °C) was evaluated and compared with two series of TFTs produced at room temperature and 150 °C during the channel deposition. From the results it was observed that the effect of pos annealing is crucial for both series of TFTs either for stability as well as for improving the electrical characteristics. The a-GSZO TFTs operate in the enhancement mode (n-type), present a high saturation mobility of 24.6 cm^2/Vs, a subthreshold gate swing voltage of 0.38 V/decade, a turn-on voltage of -0.5 V, a threshold voltage of 4.6 V and an I_{ON}/I_{OFF} ratio of 8×10^7, satisfying all the requirements to be used in active-matrix backplane.

1. Introduction

Amorphous Oxide Semiconductors (AOS) are very attractive for TFT applications, from a manufacturing point of view, because they combine simultaneously the advantages of amorphous silicon and polycrystalline silicon based TFTs. They can be produced at room or even relatively low temperatures (compatible with low cost polymeric substrates) presenting very smooth surfaces without grain boundaries (advantage for process integration). Based on these results several reports have been presented with AOS based TFTs using different system compositions like a-IZO [1-4], a-GIZO [5-8] and a-ZTO [9,10]. From the TFT analysis it is clearly observed that, in order to achieve high channel mobilities the most promising candidates are based on systems including In, in percentages higher than 40% for ternary systems. Besides that, since the availability of In is limited (is a by-product of mining ores for other metals, such as zinc, copper, lead and tin [11], existing ~ 1000 times more zinc (132 ppm) than indium (0.1 ppm) in the earth's crust [12, 13] solutions avoiding the use of In are nowadays preferable. In this work we report the fabrication of high performance oxide based TFTs by replacing the metal cation of In by Sn, using as semiconductor an a-GSZO thin film rf-cosputtered using a dual GZO and Sn targets.

2. Experimental

The TFTs were produced using heavily doped p-type silicon substrates coated with 100 nm SiO_2, which acted as the gate dielectric. A 5/75 nm thick Ti/Au film was deposited by e-beam evaporation on the backside of Si to form the gate electrode. A 50 nm thick a-GSZO layer (the semiconductor) was then deposited by r.f. magnetron cosputtering in a home made sputtering system. A 3” diameter $ZnO:Ga_2O_3$ (95:5 wt%) ceramic target and a 2” diameter Sn target from SCM were used, at a base pressure

of 3×10^{-4} Pa, an oxygen partial pressure of 1×10^{-1}Pa, a processing pressure ($Ar+O_2$) of 7×10^{-1} Pa and r.f. power of 75 and 20 W for the $ZnO:Ga_2O_3$ and Sn targets, respectively. The 200 nm thick source/drain electrodes (Ti) were e-beam evaporated top of a-GSZO. Both the semiconductor and the source/drain layers were patterned by lift-off and the produced transistors had a fixed width (W) of 50 µm and length (L) of 50 µm. Two different series of transistors, S1 and S2, were produced: in S1, the a-GSZO was produced at room temperature, while in S2 it was deposited at 150 °C. After production, both series of TFTs were annealed in a Barnstead Thermolyne F21130 tubular furnace, with a constant flow of nitrogen, at 150 °C, 200 °C, 250 °C and 300 °C.

The films thicknesses were measured with a surface profilometer Sloan Tech Dektak 3.

X-ray diffraction measurements were performed at RT in air, using the CuK_α line (λ = 1.5418 Å) of a Siemens D-500 diffractometer. The SEM analysis was done in a FEI Strata 235-Dual Beam FIB (both in surface and cross section after vertical milling using Ga ions). X-ray Photoelectron Spectroscopy (XPS) analysis was done using the Al K_α (non monochromatic) radiation of an XSAM800 (KRATOS) spectrometer operated in the fixed analyser transmission (FAT) with a power of 120 W (10 mA and 12 kV) in order to evaluate the composition and chemical states of the a-GSZO thin films as well as the chemical composition. Spectra acquisition was done without flood gun, the carbonaceous contamination (C 1s binding Energy = 285 eV) being used as reference for binding energy correction. For quantitative data treatment, sensitivity factors provided by the equipment manufacturer were used. The optical characterization of the films were measured using a UV-VIS-IR spectrophotometer (3100 Shimadzu double beam) and an ellipsometer model Jobin-Yvon UVISEL in the spectral range from 1 to 6 eV at an incidence angle of 70. We use the layer model analysis, which is based on Tauc-Lorentz dispersion with two oscillators.

The TFTs were electrically characterized in air at room temperature, in the dark using a Cascade Microtech M150 microprobe station connected to a semiconductor parameter analyser (Agilent 4155C) controlled by the software Metrics ICS.

3. Results and discussion

Figure 1 (a) shows the X-ray diffraction pattern for the a-GSZO film used at the channel layer, deposited at room temperature on corning 1737 glass substrate with a thickness of 175 nm. The two diffractograms refer to the film as produced and post annealed at 250 °C in a N_2 atmosphere, respectively. An amorphous like behaviour is observed which was also confirmed by the SEM cross section of the same film, shown at figure 1 (b). The surface morphology is also shown in the SEM image presented in figure 1c). The films present a very smooth surface with an average roughness of 0.6 nm (inferred by AFM analysis).

The results concerning the structural and morphological characterization even after annealing do not present any detectable variation. Nevertheless, the electrical measurements (not presented in this letter) are quite influenced by the annealing temperature. The resistivity for a-GSZO (measured with co-planar Al electrodes) as produced is 4.6×10^{10} Ωcm and after annealing decreases about 8 orders of magnitude to a value of $\approx1\times10^{2}$ Ωcm, with a Hall mobility (using the van der Pauw configuration) of 5 cm^2/Vs.

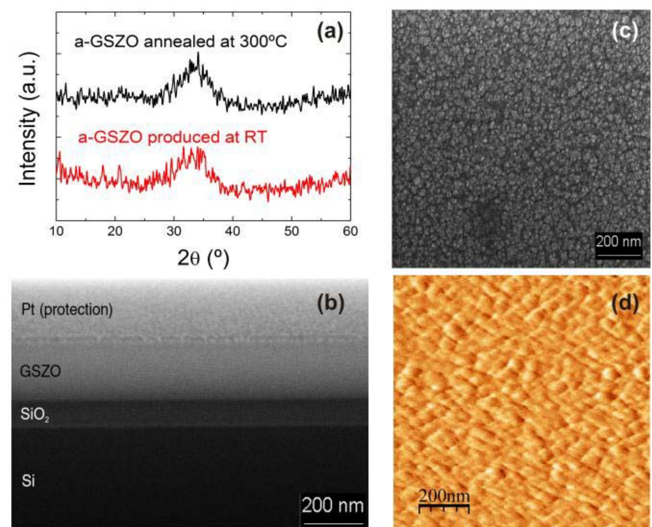

Fig. 1. Structural and morphological properties presented by a typical a-GSZO film with 175 nm thickness, produced by rf magnetron cosputtering (a) X-ray diffractogram for a-GSZO film deposited at RT and annealed at 250 °C. (b) SEM cross section of a-GSZO film deposited on SiO_2/c-Si wafer, (d) Surface morphology by SEM and (d) AFM image, presenting an average roughness around 0.6 nm.

The decrease in resistivity with increasing annealing temperature is attributed to modification of the semiconductor or to improved local atomic rearrangement, possibly related to a change in the oxidation state of Sn. With increasing annealing temperature, there is a surface enrichment in Ga and, especially in Sn. The Ga/Zn atomic ratio in samples as processed and annealed at 200 °C is 0.06 and in the one annealed at 300 ºC is 0.12. Regarding photoelectron binding energy (B.E.) of different elements, they correspond to the oxidized forms: B.E.(Ga 2p)=1118.7 ± 0.2 eV, typical of Ga 2p from Ga_2O_3 [14] and B.E.(Zn 2p)=1022.3 ± 0.2 eV typical of Zn 2p from ZnO [15]. Concerning Sn, its photoelectrons Sn 3p and Sn 3d present, in all the samples, binding energies of 716.1 ± 0.2 and 486.2 ± 0.2 eV, respectively which can be assigned either to SnO or SnO_2 given their binding energy proximity and the

dispersion of values in literature. A more robust parameter, independent of charge accumulation correction, is the modified Auger parameter which is, for all the samples, 918.3 ± 0.2 eV which is closer to the SnO_2 modified Auger parameter than to the SnO one [29]. O 1s peak is fittable with two components centered at 530.4 ± 0.2 eV and at 532.1 ± 0.2 eV assignable, respectively to the oxide and hydroxide oxygen forms. The ratio O(oxide)/O(hydroxide) increases with the annealing temperature increase. Another indirect result from XPS data concerns spectra charge shifts which were 9.5, 8.5 and 4 eV for RT, 200 and 300º C, respectively. This is an indication that the number of hole traps in the samples decrease with the annealing temperature.

The refractive index and the extinction coefficient are presented in figure 2 for a polycrystalline GZO (obtained by rf sputtering from a ceramic target of 95% ZnO:5%Ga_2O_3 [16]) and for an a-GSZO thin films.

Near the band gap energy (3.6 eV) the GZO thin film exhibits a sharpest peak associated to an abrupt variation of the extinction coefficient. By comparing both films the GZO has a higher refractive index in the transparent region except for higher energies where a-GSZO presents a higher refractive index. Concerning the extinction coefficients (figure 2 (b)) a-GSZO presents a higher threshold energy than that of GZO. These results have also been observed for the case of a-GIZO (Ga-In-Zn-O) thin films [17].

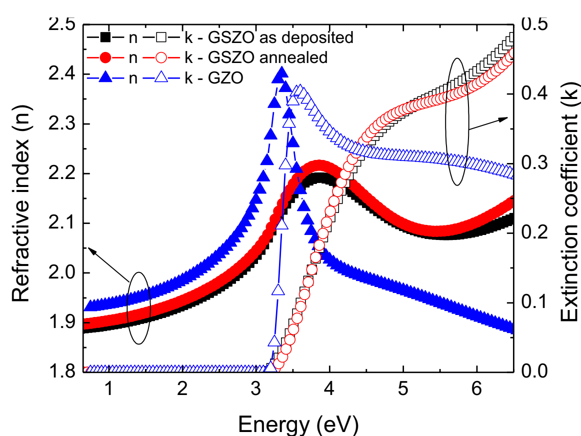

Fig. 2. Comparison of (a) refractive index and (b) extinction coefficient of GZO and GSZO thin films.

Figure 3(a) and (b) represent the two series (S1 and S2) of electrical characteristics of a-GSZO TFTs at drain-source voltage of 20 V (saturation region), produced at room temperature and 150 °C, respectively and both post annealed after production at 300 °C. The obtained results are quite similar for the two series of TFTs, presenting S2 slightly improved performance, mainly related to the increase on the saturation mobility to values of the order of 25 cm^2/Vs. In table I it is performed a comparison of the electrical parameters extracted for the two series of a-GSZO TFTs after each annealing temperature stage.

The data reveals a drastically improvement of the electrical properties for both series of a-GSZO TFTs. For S1 TFTs they start to work only for annealing temperatures higher than 250 °C while for S2 TFTs, even though they work after production, the electrical behavior is not stable (for successive and repeated measurements a positive V_{on} shift is observed, which should be related with electron trapping at (or near) the insulator-semiconductor interface). Only after annealing at 200 °C the S2 TFTs present stable and reproducible electrical characteristics. Concerning saturation mobility, μ_{sat} (calculated by the derivative of the $\sqrt{I_{DS}}(V_{GS})$ plot with V_{DS}= 20 V) an increase is observed as the annealing temperature increases, for the two series of TFTs analyzed, with a maximum value of the order of 25 cm^2/Vs, for films processed with an initial temperature of 150 °C. This improvement with annealing temperature is attributed to modification of the semiconductor/insulator interface with temperature and/or to improved local atomic rearrangement [9] as it was confirmed by XPS analysis.

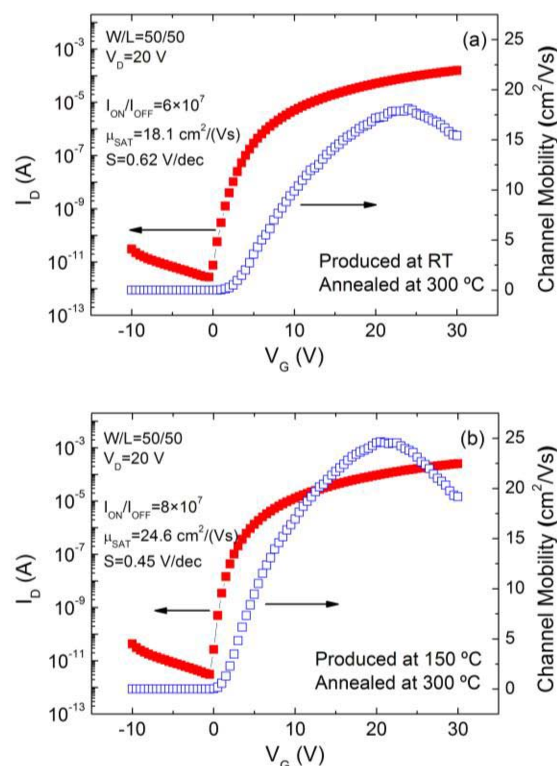

Fig. 3. I_D–V_G transfer characteristics obtained at V_D = 20 V (saturation region) for a-GSZO TFT produced at (a) room temperature (S1) and (b) produced at 150 °C (S2). Both devices were post annealed at 300 °C in a nitrogen atmosphere for 1 h. The saturation mobility, μ_{sat} was calculated by the derivative of the $\sqrt{I_{DS}}(V_{GS})$ plot with V_{DS}= 20 V.

The threshold voltage, V_{th} is almost independent of the initial processing conditions as well as of the annealing temperature, remaining an average value of 5 V. The I_{ON}/I_{OFF} ratio for the S1 series increases by factor of 3 (from 250 to 300 °C), while for S2 series an increase is observed from 200 to 250 °C (from 3×10^8 to 7×10^8) and a decrease for 300 °C (8×10^7). A different behavior is observed for the sub-threshold voltage swing (S). For TFTs from series S1 a decrease is observed in S, from 0.75 to 0.62 V/decade, suggesting a better interface when the devices are annealed at higher temperatures. On the other hand, for the TFT from series S2 an opposite dependence is observed, as the annealing temperature increases from 250 to 300 °C. Here, a deterioration of the S value is observed, from 0.38 V/decade to 0.45 V/decade.

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4. Summary

In summary we have demonstrated the possibility to produce high performance oxide based bottom gate TFTs replacing the In by Sn in the Ga-Zn-O system, which is an important advantage due to the limited availability of In. The morphological and structural characteristics have been determined, revealing very smooth surfaces, typical for amorphous materials. XPS analysis reveals a segregation of Ga^{3+} and specially of Sn^{4+} at the surface induced by annealing. The device electrical characteristics are drastically improved when the TFTs are subjected to a post annealing treatment, with an optimal temperature of 300 °C, without changing the amorphous structure of the multicomponent semiconductor. The annealing treatment dominates device characteristics and minimizes the effect of other process parameters. The performances of the a-GSZO presented in this letter are comparable and in some cases superior than those of a-GIZO TFTs.

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