Transparent-Oxide-Semiconductor Based Staggered Self-Alignment Thin-Film Transistors

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Abstract

Staggered type self-aligned transparent-oxide-semiconductor transistors with indium-zinc-oxide as a semiconductor have studied. In this device fabrication, successive sputtering of oxide semiconductor and insulator without breaking of vacuum and without exposing in air, humidity and oxygen can be realized because oxide semiconductor is transparent. As a result of fabrication, transistor characteristics with mobility of 30cm^2/Vs and on-off ratio of 10^5 could be obtained for the newly developed self-alignment device structure.

1. Objectives and Background

Study on transparent-oxide-semiconductor thin film transistors (TOSTFTs) is actively carried out[1-3] and recently an integrated circuit is also fabricated.[4] Here, a reduction of a parasitic capacitance is necessary for a reduction of the charge sharing and higher operational speed for the integrated circuit as a backplane. In this time, we have studied a staggered self-alignment (SA) TOSTFT with a top gate structure where a back surface exposure is applied after semiconductor layer sputtering by using transparent IZO as the semiconductor layer.[5,6]

2. Results

Figure 1 shows process steps of the SA-TOSTFT under study. First, source/drain electrode was deposited on a glass substrate and was patterned using reactive ion etching. Second, semiconductor layer were sputtered and was annealed at 110℃ for 1h. Then, a gate insulator was deposited and the semiconductor and gate insulator were patterned and etched. After then, back-surface exposure was carried out, where the source/ drain electrodes were used as a photomask. Next, a gate electrode was evaporated and a lift-off process was carried out. After lift-off process, overlapping length between gate and source/drain electrodes was as small as 0.5 μm. Therefore, reduction of parasitic capacitance will be expected. After lithographic process, the gate electrode was etched off.

Figures 2 and 3 show drain voltage vs drain current characteristics and gate voltage vs drain current characteristics, respectively. Channel length and width were 50 and 150 μm, respectively. Field-effect mobility (μ_{FE}) of 30 cm^2/Vs was obtained. From Fig. 3, n-channel depletion transistor characteristics with on/off ratio of 10^5, threshold voltage of -7 V was obtained.

3. Impact

Staggered-type self-aligned oxide-semiconductor transistor with top-gate structure was achieved by applying back-surface exposure for the first time. In this structure, oxide semiconductor was transparent. Therefore, the back-surface exposure process can be done after sputtering of oxide semiconductor and gate insulator. In addition, transistor fabrication process is carried out without breaking of vacuum, i.e., without exposing in air, humidity and oxygen. With these characteristics, superior and feasible SA-TOSTFT is realized for integrated circuit and back-plane.

4. References

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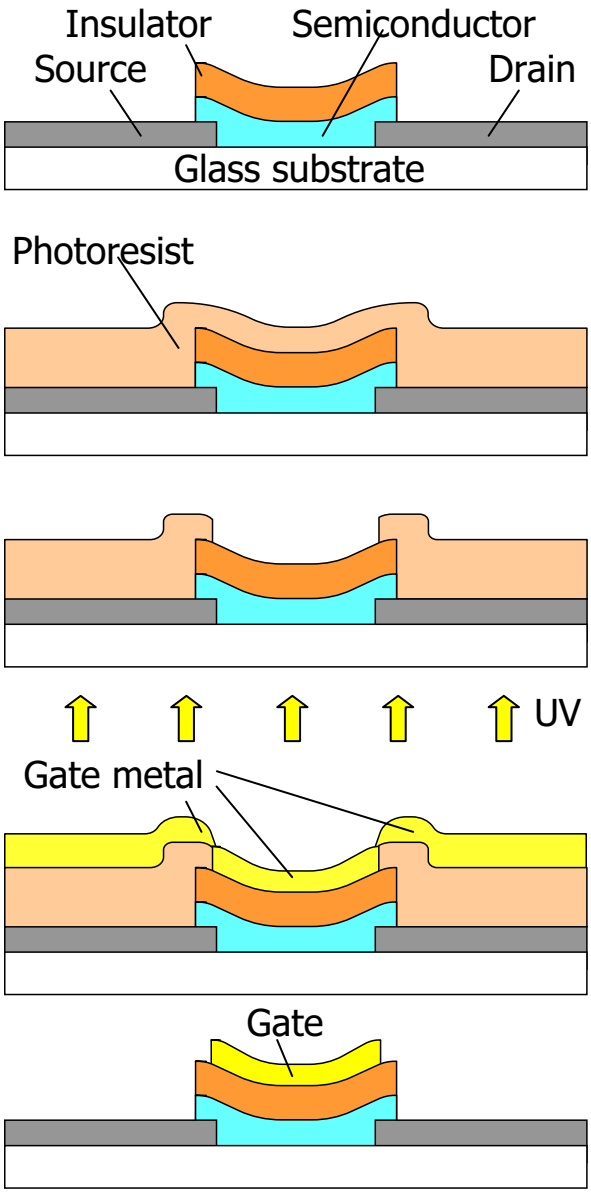

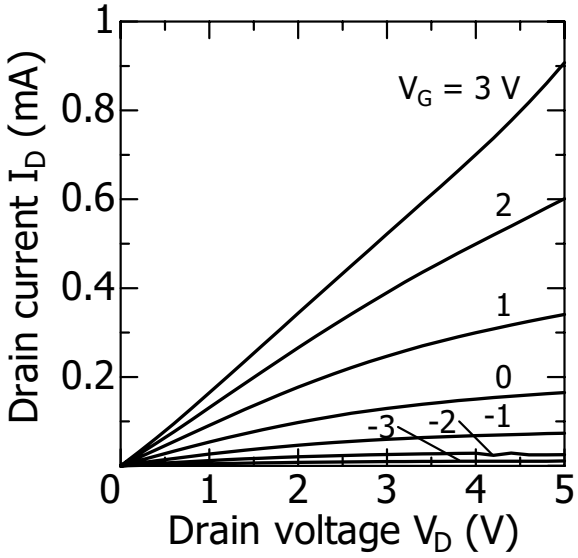

Fig.2 Drain voltage vs drain current characteristics.