Optimization of a-IGZO Thin-Film Transistors for OLED Applications

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Abstract

We demonstrate that the performance of amorphous indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFT) can be optimized by controlling the interfaces between IGZO and sandwiching insulators and by proper deposition of IGZO layer. Specifically, contact and channel resistances are decreased by reducing IGZO bulk resistance and optimizing dry-etch process, respectively. Field-effect mobility ($_{FE}$) and subthreshold gate swing (S) are further enhanced by fine-tuning IGZO deposition condition.

1. Introduction

Amorphous indium gallium zinc oxide (IGZO) TFTs have gained much attention as an attractive alternative to poly-Si TFTs to drive organic light-emitting devices (OLEDs) due to their excellent device uniformity and a high mobility [1-4]. Specifically, IGZO TFTs are free from the non-uniformity of the mobility and threshold voltage that stems from the grain boundaries of poly-Si TFTs because of their amorphous nature. Their large charge carrier mobility (> 10 $cm^2/V\cdot s$) and excellent subthreshold gate swing (0.20V/dec) are sufficient to drive large-area AMOLEDs. For example, our recent demonstration of the 12.1" WXGA AMOLED display [5] shows that IGZO TFTs are promising for large-size application such as note PC and HDTV because IGZO semiconductor can be deposited on large glass substrate (>Gen. 7) using conventional sputtering system.

In this paper, we demonstrate some practical solutions to optimize a-IGZO TFTs. For example, contact and channel resistances, which limit the μ_{FE}, are decreased by reducing IGZO bulk resistance and optimizing dry-etch process, respectively. The S value can be reduced by minimizing back-channel corruption from the deposition of etch stopper layer (ESL). The μ_{FE} and S values are further enhanced by fine-tuning of IGZO deposition condition.

2. Experimental

Lithographically patterned Mo (200nm) on a SiO_2/glass substrate with a surface area of 370×400 mm^2 was used as the gate electrode. Either SiOx film or SiOx/SiNx bi-layer film as a gate dielectric layer was deposited by plasma enhanced chemical vapor deposition (PECVD). The 50 nm a-IGZO film was grown by sputtering on the SiO_2/glass substrate using a polycrystalline $In_2Ga_2ZnO_7$ target at room temperature. After defining the a-IGZO channel using photolithography and wet etching, ESL was deposited by PECVD and then, patterned by dry etching. As a source and drain electrode, either Mo or Ti/Al/Ti material was formed by sputtering and defined by photolithography and then patterned by dry etching. The device characteristics of the a-IGZO TFTs were measured at room temperature with an Agilent 4156C precision semiconductor parameter analyzer.

3. Results and discussion

3.1. IGZO TFT: Contact and channel resistances

Figure 1 illustrates the schematic cross-section that describes an IGZO TFT at the operating state. When the gate is positively biased, electrons are accumulated at the narrow region near the GI/IGZO interface, resulting in the channel formation. The

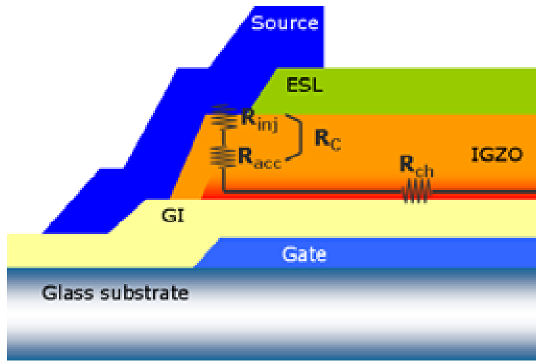

Fig. 1. The schematic cross section showing the contact (R_C) and channel (R_{ch}) resistances.

apparent field-effect mobility induced by the transconductance at a low drain voltage (V_{DS}<1V) is determined by

$$\mu_{FE} = \frac{Lg_m}{WC_iV_{DS}}, \qquad (1)$$

where L, W, C_i and g_m are the channel length, width, the gate capacitance per unit area and the transconductance, respectively. [6]

In order to maximize the μ_{FE}, TFT resistance should be minimized. The total resistance R_T is the addition of the contact and the channel resistances, R_c and R_{ch}, respectively. The R_c is comprised of the injection and the access components, R_{inj} and R_{acc}, respectively. The R_{inj} comes from the energy barrier for electrons travel from source metal to IGZO, thus it is intrinsically determined by the work function difference between two materials. Once electrons are injected to IGZO, they feel the additional resistance R_{acc} until they reach the channel region. The R_{acc} can be alleviated by reducing the bulk resistance of IGZO. In fact, we have previously shown that the R_{acc} is controlling factor to determine R_c in IGZO TFTs. [7,8] The R_{ch} value is mainly determined from the quality of GI/IGZO interface because the channel is typically formed at the very thin region near the interface.

The R_c and R_{ch} values can be decoupled by following method. Because R_{ch} is proportional to L and R_c is independent, R_T can be described as

$$R_T = R_{ch} + R_C = \frac{R_{ch}'}{W}L + R_C \qquad (2)$$

where the unit of R_{ch}' is [/sq] and the others are [ ]. Therefore, the R_{ch}' and R_c can be obtained from the slope and the y-intercept of a R_T vs. L plot.

3.2. GI/IGZO interface optimization

The reduction of the contact and the channel resistances can be achieved by reducing the bulk resistance of IGZO layer and by reducing the traps at the GI/IGZO interface, respectively. To prove this hypothesis, we designed a set of experiment using high (A) and low (B) resistance IGZO and 1- and 2-step dry etch process.

The A and B IGZO were deposited from different sputter targets. At the identical film thickness, the sheet resistance values were differed as two to three orders of magnitude. Interestingly, the R_CW values were about an order lower for B at the same etch condition whereas R_{ch}' is only 5~18% lower.

In order to optimize the GI/IGZO interface, we developed a 1-step dry etch process of GI and ESL. In this process, the GI and IGZO layers are sequentially deposited by skipping GI patterning, thus the corruption of GI/IGZO interface can be mitigated. The 1-step etch process resulted in the 35~45% reduction of R_{ch}'. The reduction of R_CW can be attributed to the overetch of IGZO from the 1-step etch. It is notable how the reduction of R_CW and R_{ch}' results in the enhancement of μ_{FE} values.

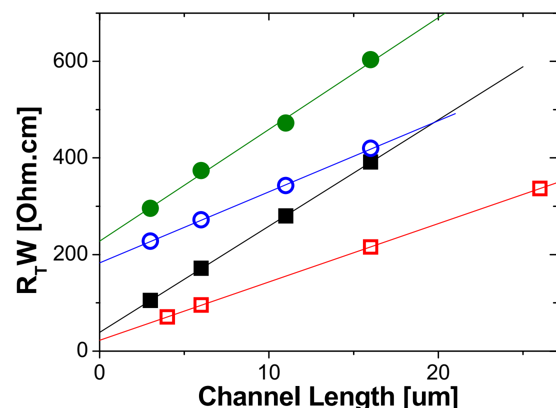

Fig. 2. The R_TW vs. L plots (at V_{gs} =20V and V_{ds}=0.1V).

TABLE 1. Legends and parameters from Fig. 2.

	IGZO	Etch	R_CW	R_{ch}'	μ_{FE}*
●	A	2-step	227.6	2.32×10^5	6.24
○	A	1-step	183.1	1.47×10^5	10.38
■	B	2-step	38.9	2.20×10^5	7.82
□	B	1-step	22.7	1.21×10^5	14.60

* The μ_{FE} values are from W/L = 29/10

3.3. IGZO/ESL interface optimization

In order to reduce the power consumption of an AMOLED, The subthreshold gate swing (S) should be minimized. From the transfer characteristics, the S value can be extracted using the equation

$$S = \frac{dV_{gs}}{d(\log I_{ds})}. \tag{3}$$

Because the charge accumulation at the channel layer is not fully achieved at the subthreshold region, the S value is dependent on the back-channel (IGZO/ESL) trap density, as well as the bulk and channel (GI/IGZO) trap densities.

In Fig. 3, transfer curves from the optimized and non-optimized ESL deposition conditions, C and D, respectively, are compared. Except the ESL deposition condition, all the other processes were identical. As can be confirmed in Table 2, the S value of the sample C is significantly larger than that of D. Therefore, one can conclude that the minimization of back-channel damage by proper ESL deposition is necessary to optimize subthreshold property of IGZO TFTs.

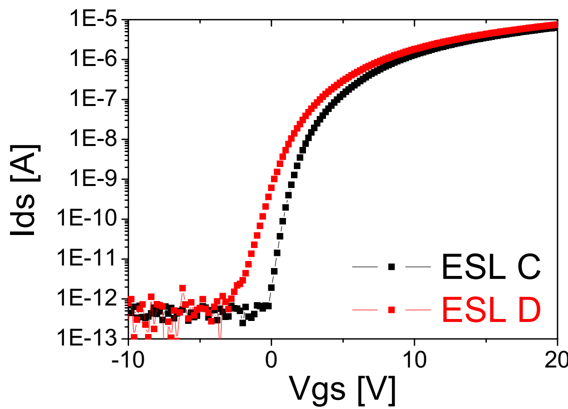

Fig. 3. Comparison of the transfer curves from two different ESL deposition conditions, C and D (W/L = 9/20 and V_{ds} = 5.1V)

TABLE 2. Parameters from Fig. 3.

	$V_{th, sat}$*	μ_{FE}	S	Ion / Ioff
ESL C	2.43	6.97	0.54	1.90×10^7
ESL D	1.68	8.89	0.82	1.93×10^7

* Defined by V_{gs} at I_{ds} = 10nA × L/W

3.4. IGZO deposition condition optimization

It is well known that the oxygen gas ratio during the IGZO sputtering process may drastically affect the TFT performance by changing carrier concentration. [9] In Fig. 4(a), the effect of oxygen gas ratio on the contact and channel resistances are illustrated. As oxygen ratio increases from 15% to 60%, both R_CW and R_{ch}' increases monotonically, which is consistent with the decreasing carrier concentration in IGZO. Consequently, the μ_{FE} values decreases from 16.3 to 12.9 at the respective oxygen ratio. However, it is notable that the R_CW value increases nearly twofold (from 22.3 to 43.0 .cm) whereas the change in R_{ch}' is only 10% (from 115 to 128 K /sq). This strongly suggests that the channel layer is narrowly confined near the GI/IGZO interface, thus the R_{ch}' is a strong function of the interface property whereas it is less sensitive to the IGZO quality. (See Fig. 2 and Table 1 to recall the effect of GI/IGZO interface optimization on the R_{ch}' reduction.) On the other hand, the contact resistance changes drastically by IGZO deposition condition. Finally, a monotonic decrease of S value is observed with increasing oxygen ratio. The origin of the improvement requires further investigation.

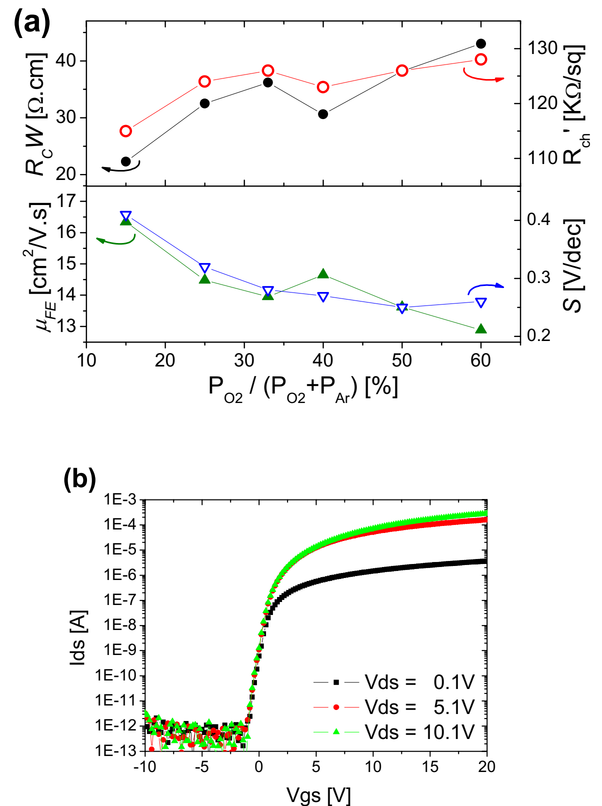

Fig. 4. (a) The variations of R_cW, R_{ch}', μ_{FE}, and S of the IGZO TFTs as a function of oxygen ratio during the IGZO deposition process. (b) Corresponding transfer curves at the oxygen ratio of 40%. (W/L = 29/8)

4. Summary

In this paper, we have shown that the performances of IGZO TFTs can be optimized by tuning the process condition. Here, we categorized the TFT by three parts, namely, charge injection part (associated with R_C), channel part (associated with R_{ch}), and back-channel part (associated with ESL deposition). The quality of charge injection part was shown to improve with the proper choice of IGZO deposition condition. The quality of channel part was mainly determined by the GI/IGZO interface, and the IGZO deposition condition also had a minor contribution. Finally, we showed the importance of the minimization of back-channel damage during the ESL deposition.

5. References

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