Data Line Sharing in TFT-LCD with the Integrated Gate Driver

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Abstract

We have succeeded in producing the world 1st TFT LCD panel adapting the data line sharing method. In the data line sharing structure, two neighboring pixels share one data line. We also adapted time shared data driving with a-Si TFT based circuit integration technology of LG Display's own. By using these technologies, we can reduce the number of source driver ICs by half, compared to that of the existing gate driver integrated TFT LCD panel.

Keywords *: a-Si TFT, Data line sharing, integrated gate driver*

Introduction

Amorphous Silicon (a-Si) technology is very suitable for large area display application. Because it has low-cost, low processing temperature, and better uniformity even in large area applications. So, it is widely used as a switching device of pixel elements in active matrix liquid crystal display (AMLCD).

Integrating driver IC on the panel is getting more important in LCD technology, because it can reduce the cost of driver ICs and the number of module processes.

For a long time, it has been regarded the two things make the a-Si TFT based gate driver integration impractical. One is that a-Si TFT has low mobility, so the widths of the TFT should extend to a degree of thousands of microns. The other is the instability of a-Si TFT. The threshold voltage of a-Si TFT is shifted due to applied bias voltage during the operation. The insufficient life-time of circuits has been the critical barrier to prevent a-Si TFT drivers from the technology used in TFT LCD mass-production. [1,4]

We have developed LGD's own integrated a-Si gate driver with extreme stability as indicated by our previous papers. [2,3]

Recently, a few companies also have succeeded in mass-producing the LCD panel with the integrated gate-driver IC. By making the integrated gate-driver by conventional a-Si TFT as same as the pixel TFT, they can reduce the cost of driver ICs and the number of module processes.

In these days, to widen the application of a-Si integrated gate driver, we have concentrated on the reduction of the area of the unit integrated gate driver and also enhancement of the output characteristics of gate driver. As the results of our research, we can achieve the world's 1st mass production of 14.1 WXGA TFT-LCD panel with integrated gate driver and 50% of source driver ICs.

DLS : Reduction of Source Driver IC

To reduce the number of source driver IC, we should change the date - pixel - gate structure. By using data line sharing(DLS) structure, we could reduce the half of the source driver ICs. Fig.1 shows the schematic diagram of DLS structure. Two neighboring pixels share the same data line with each gate line and pixel TFT. So, total number of gate line increases double as that of the conventional pixel structure.

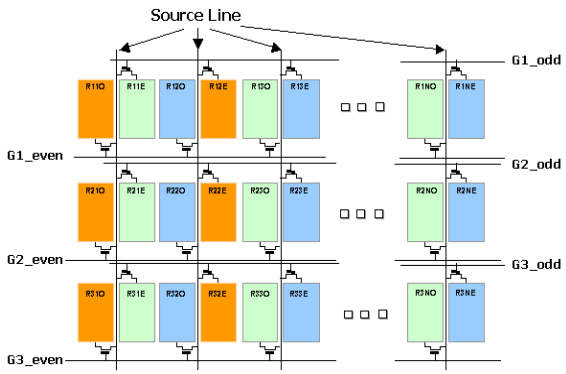


Fig. 1. Schematic diagram for Data line sharing (DLS) structure

It also means the height of unit integrated gate driver decrease the half of the original pixel height.

In the view point of the operating timing, the charging time of each pixel reduces into the half of the conventional by adopting the DLS structure. Fig.2 is the simple timing chart for this DLS technology.

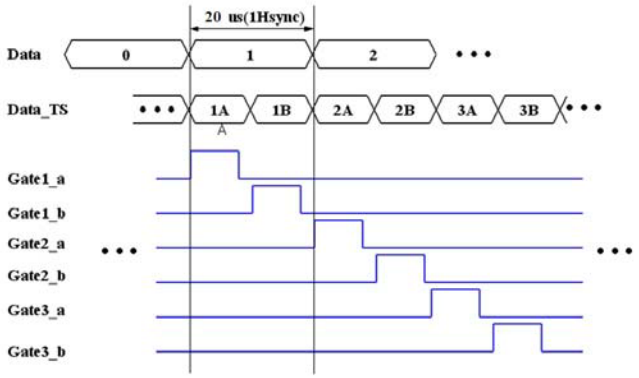


Fig. 2 Signal diagram for the DLS structure

There are so many diversities in DLS structures. We have investigated several pixel rendering structures, and found two kinds of pixel structures. Using the one of them we could achieve the mass production of the TFT-LCD panel for NBPC. Fig.3 is the typical two type of pixel rendering in DLS pixel structures. During development period, two types have been shown little differences in their display properties.

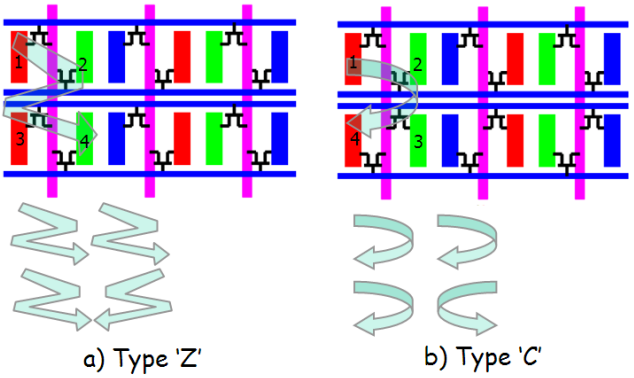
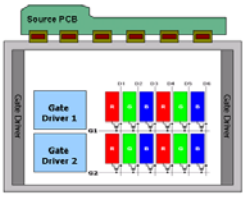
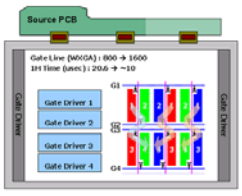


Fig. 3 Schematic diagram for the typical pixel rendering structure in DLS technology

Improvement of the performance of integrated gate drivers

By adapting DLS structure, almost 4 times of output properties are needed. The area where we can integrate the driver reduces into half by double gate lines (800ea. → 1,600ea.). And, the pixel charging time (1H time) is decreased into 50% by data line sharing (20us → 10us). TABLE.1 shows that situations.

TABLE 1. Comparison of integrated gate driver and DLS with integrated gate driver

Integrated Gate Driver	DLS with integrated Gate Driver
1280xRGBx800	1280xRGB/2 x 800x2
	
Gate D-IC: 2ea → 0ea Data-DIC: 6ea (640ch)	Gate D-IC: 2ea → 0ea Data-DIC: 6ea → 3ea (640ch)

As below equation, the output current of the buffer TFT is directly proportional to the performance of integrated gate driver.

$$I_{output}\ \alpha \left(\frac{W}{L}\right)\cdot \mu$$

W : channel width
L : channel length
μ : mobility

The output current is proportional to the channel width and the mobility of the TFT. So, to guarantee the performance of integrated gate driver in DLS structure, we adopted our genuine gate driver schematic, Hyper Dual AC structure (HDAC). And we also adopted shorten the length of TFTs to improve the performance of unit TFT.

A. HDAC circuits.

From our previous works, we have already developed the integrated gate driver with extreme stability. The main idea for the extreme stability is the dual pull-down structure (DAC). And, this LGD's own circuit is adopted into the TFT-LCD production. Fig. 4 is the basic diagram and QB timing for DAC circuit.

But, to achieve the upgrade the performance of integrated gate driver, we developed several QB node sharing technology and confirmed its reliability is

comparable to the current DAC type gate driver.

In this work, we adopted hyper DAC structure (HDAC). Table 2 shows the comparison the concepts of HDAC and DAC. HDAC is the QB sharing technology which vertically neighboring two gate driver share their QB nodes and reduce 2 sets of QB node control TFTs. [5,6]

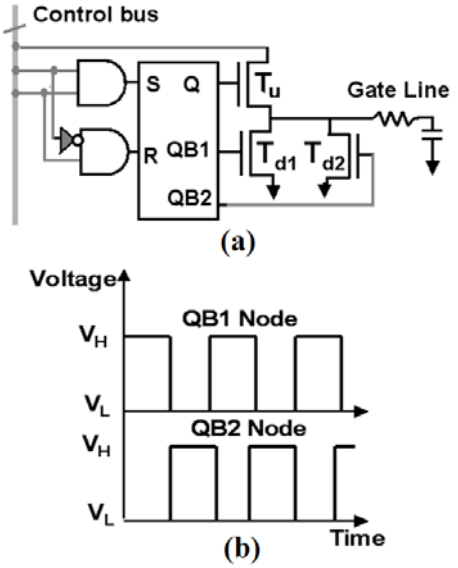


Figure 4. (a) Schematic block diagram of gate driver circuit with the dual pull-down (DAC) TFTs structure and (b) timing diagram of two QB-nodes of gate driver

TABLE 2. Comparison of the sharing type of DAC and HDAC GD

GD type	DAC	HDAC
Sharing Node	none	QB1(●) , QB2(●)
	GD N GD N+1 GD N+2 GD N+3	GD N GD N+1 GD N+2 GD N+3
TFT Numbers of a unit GD (relative.)	100	< 50
Area of a unit GD (relative value)	100	< 70

With this HDAC gate driver, we could successfully integrate gate driver into 50% area and operate faster in double rates in 14.1 WXGA TFT-LCD. Via qualification processes at various companies, the reliability of this panel has successfully approved.

B. Short Channel TFT.

To secure the stable performance of integrated gate driver, we should enhance the output characteristics of a-Si TFT. By reducing the TFT's channel length from 6um to below 5um, we could achieve the ~15% of improvement in the output current, and also can cover the variation of TFT characteristics which can occur during the mass production. So, we experienced no loss in the yield of the TFT-LCD production in this 14.1 WXGA TFT-LCD with DLS technologies.

C. Low resistance of metal line

In DLS structure, the number of pixel TFTs which connected to 1 data line becomes twice. So, the data line load increased. By decreasing the resistance of data line metal, we could solve the data line delay issues. And, also by adapting low-resistance gate line, we could get a lower gate delay. Fig 5. shows the measured output of gate driver of this work. By adopting low resistance metal lines (gate line & data line) we could reduce ~ 0.4us of falling time.

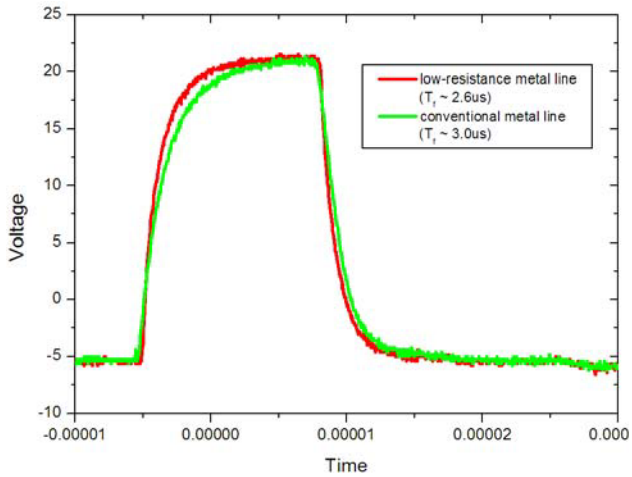


Figure 5. The measured output characteristics of integrated gate driver in 14.1" WXGA TFT-LCD with DLS technologies.

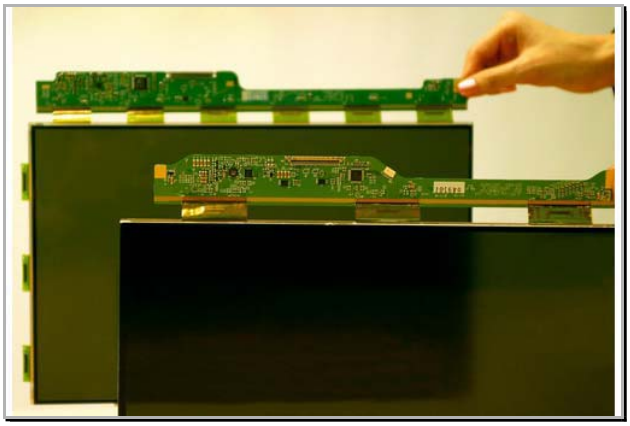


Figure 6. The comparison between the normal LCD panel and the DLS LCD panel (LG Display's 14.1" WXGA NBPC : The world 1st mass production)

Summary

We presented the integrated a-Si gate driver for DLS(data line sharing), by which only three 640-channel data driver ICs are needed in 14.1" WXGA (1280X800) TFT-LCD Panel. The 14.1" WXGA panel adopting the integrated gate driver was successfully developed and it was the world's 1st mass production of TFT-LCD panel with a-Si TFT gate driver and halved source driver ICs.

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