Quad-functional Built-in Test Circuit for DRAM-frame-memory Embedded SOG-LCD

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Abstract

A quad-functional built-in test circuit has been developed for DRAM-frame-memory embedded SOG-LCDs. The quad function consists of memory test, display test, serial transfer test, and parallel transfer test which is the normal operation mode for our SOG-LCD. Results of memory and display tests are shown.

1. Introduction

In system-on-glass (SOG) displays, a lot of circuits are integrated onto displays using polycrystalline silicon thin-film transistors (poly-Si TFTs). As a first step to realize a Zero-chip display, which needs no external IC and connects directly to the CPU bus, we reported about a DRAM-frame-memory embedded SOG-LCD (See Fig.1) [1]. This previous work represents the first successful SOG-LCD, which integrates a DRAM frame memory in a picture frame area on the glass substrate.

Testing it is not what it used to be. Before DRAM integration, the display and DRAM were separately tested. After the integration, however, there arose difficulty in testing each part separately. To realize testability, which consists of controllability and observability, many control points (CP) and observation points (OP) should be inserted. Figure 2 shows the primitive implementation of testability in DRAM-frame-memory embedded SOG-LCD. The OP for the display area is realized by the display area itself. Three other system blocks, CP for display, OP and CP for memory, are newly added. In addition, a functional test block for each CP and OP is needed. These newly added system blocks make the circuit area larger and increase the possibility of defects appearing. In this paper, we describe a simple and small-footprint implementation of a built-in test circuit with quad functions for DRAM-frame-memory embedded SOG-LCD.

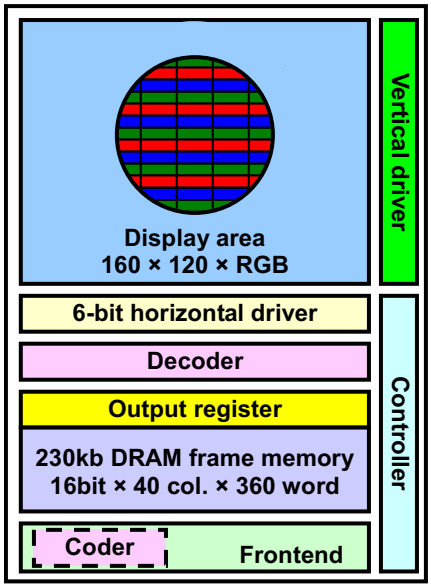

Fig. 1 System block of the DRAM-frame-memory embedded SOG-LCD.

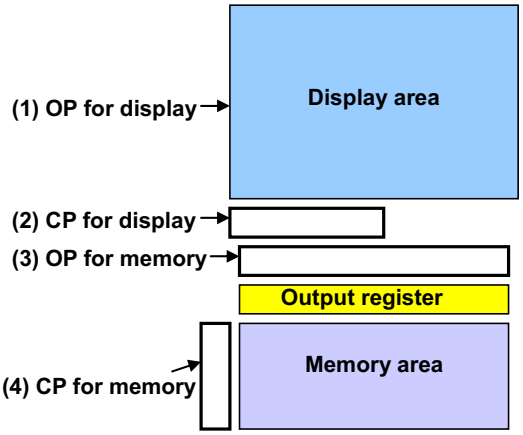

Fig. 2 Primitive implementation of testability in the DRAM-frame-memory embedded SOG-LCD.

2. DRAM-frame-memory embedded LCD

Figure 1 shows a system block of our LCD presented in Ref. 1. Input image data are written to the frame memory through the frontend, where the original 18-bit/pixel data (R:G:B=6:6:6) are transformed into 12-bit/pixel (r:g:b=4:4:4) by the coder [2]. The data are read from the frame memory in synchronization with the display timing. All the bitlines of the frame memory are connected to the output register so that all data corresponding to one horizontal line on the display are read in single row access. The stored data in the output register are transferred to the decoder, where the data are decompressed to 18-bit/pixel. Then, the data are transferred to the horizontal driver including 6-bit DACs to write analog gray-scale voltages to pixels.

3. Circuit implementation

A. Output register modified to built-in test circuit

Instead of the conventional output register in Fig. 1, a quad-functional built-in test circuit is implemented. In the primitive implementation in Fig. 2, the output register consists of latches and the CP for memory normally consists of shift registers. Our basic idea for small footprint is to combine these two circuits by using shift register latches (SRLs). In the SRL, shift register function and latch function can be selected. This SRL is widely used in the scan design of the conventional IC testing and enables two functions; one is the normal operation and the other is the scan test. In our design, four functions, which consist of memory test, display test, and two self-tests, are realized by a single built-in test circuit.

B. Circuit element

The multiplexed input flip-flop in figure 3 is used as a circuit element for our built-in test circuit. This circuit has a multiplexer function in the data and clocks. The clock multiplexers are not shown in Fig. 3.

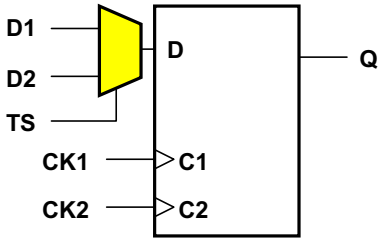

Fig. 3 Multiplexed input flip-flop.

This type of flip-flop is functionally identical to the flip-flop in the conventional scan-path test technique [3]. Using a plural number of these flip-flops in serial connection, the shift register is formed. In parallel connection, the array of parallel latches is formed.

Two data, D1 and D2 are used. Two clocks, CK1 and CK2 are in non-overlapping phases. These CK1 and CK2 can be selected from system clocks or test mode clocks. When TS is low, D1 is latched and transferred to Q. On the other hand, when TS is high, D2 is latched and transferred to Q. The output Q is connected to both the D1 of the next flip-flop and the decoder. D2 is connected to the memory output.

C. Quad functionality of the built-in test circuit

As for the built-in test circuit, three functions, (1) memory test, (2) display test, (3) self test, are required. Our implementation method for these three functions and additional one function is shown in figure 4. These four functions are realized by the combination of the two inputs, in serial or parallel, and the two outputs, in serial or parallel of our test circuit.

Fig. 4 (a) shows a data transfer image for memory test operation. In the memory test, the flip-flops are serially connected and data read from the memory is latched at our test circuit and serially put out to the outside. Thus, the CP for this operation is the latching point of the test circuit and the OP is the outputting point of the test circuit.

Fig. 4 (b) shows a data transfer image for display test operation. In the display test, the flip-flops are serially connected and data are input directly to the test circuit and output to the display area. Therefore, the CP for this operation is the inputting point of the test circuit and the OP is the display area itself.

Fig. 4 (c) shows a data transfer image for the serial data transfer test. In the serial data transfer test operation, the flip-flops are serially connected and data is input directly to the test circuit and put out to the outside. Thus, the CP for this operation is the inputting point of the test data and the OP is the outputting point of the test circuit. This mode is the self-test mode for the serial data transfer of our test circuit.

Fig. 4 (d) shows a data transfer image for the normal operation and parallel data transfer test operation. In the normal operation, the flip-flops are not connected to each other, and used in parallel. Data read from the memory are latched at our test circuit and transferred in parallel to the display area. Thus, the CP for this operation is the latching point of the test circuit and the OP is the display area itself.

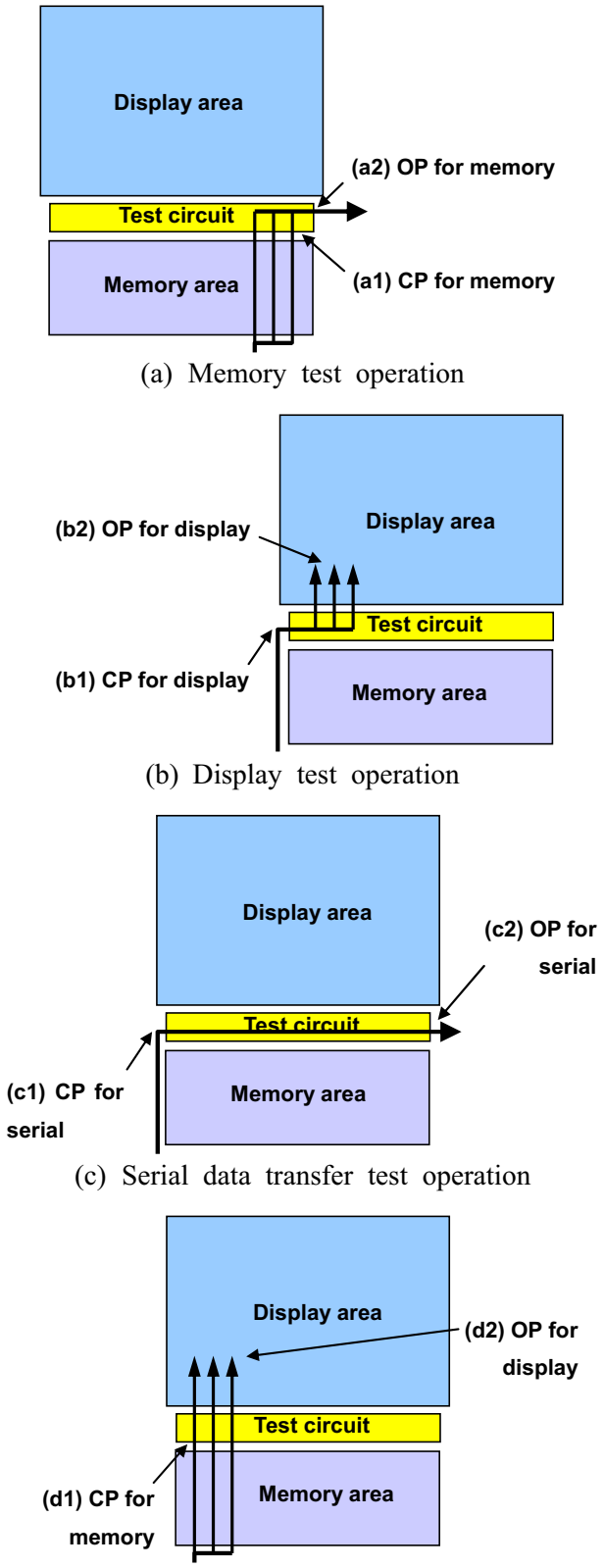

Fig. 4 Quad functionality of our built-in test circuit.

Since the test circuit is connected to the memory output directly, the output data in the memory test (Fig. 4 (a)) are the coded data. In addition, as the test circuit is inserted between the memory and decoder, the input data in the display test (Fig. 4 (b)) should be the coded data.

D. Simple structure and small footprint

The display area is a matrix-like analog memory array, where one transistor, a storage capacitor and a liquid crystal capacitor are formed within each memory cell. In the conventional testing done by array tester, analog data input is needed because the pixel is an analog memory. In the conventional SOG-LCD, even though the digital data drivers are integrated, the built-in inspection circuit is inserted between display area and digital data driver, which has the almost same function as the 6-bit horizontal driver in Fig.1 [4]. Thus, the analog readout is necessary to test the display area in the conventional SOG-LCD.

In our DRAM-frame-memory embedded SOG-LCD, the built-in test circuit is placed between the frame memory and the decoder in front of the horizontal driver. Input data for the test circuit are coded digital data. The testing of the pixel circuits is done by the optical method, thus there is no need to measure the analog signals in the test circuit. Our design without analog readout switches realizes a small footprint and reduces picture frame. Table 1 summarizes the effect of the footprint reduction of our test circuit compared to the primitive implementation in Fig. 2.

TABLE 1. Footprint reduction of our design

	Our design	Primitive (Fig. 2)
Number of flip-flops	640	1280
Reduction of number of transistors	Around 15,000	-
Circuit height	1.3mm	2.3mm

4. Circuit operation examples

Using the developed built-in test circuit, function tests were performed.

A. Operation frequency of embedded frame memory

Figure 5 shows data failure rate versus operation frequency in the embedded DRAM frame memory. It was done by comparing the write data to the memory and the read data from it. The readout data are the

coded data, thus before comparison we performed decoding of the readout data. The result shows that the failure rate is completely zero up to the operation frequency of 1MHz.

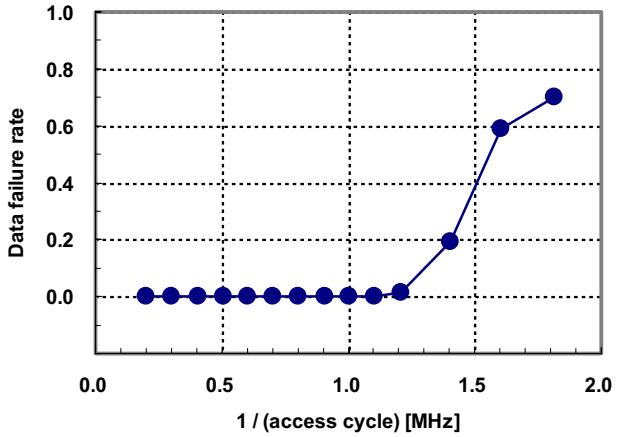

Fig. 5 Measured data failure rate vs. operation frequency in the embedded frame memory.

B. Retention time of embedded frame memory

The retention time, which is an important characteristic of DRAMs is evaluated as well. Fig. 6 shows the measured data failure rate versus retention time. It shows that the failure rate is completely zero up to 166ms retention time. Thus, a periodic reading access to display, in which the vertical frequency is over 6Hz, is all the access that is needed to refresh the memory cell to ensure the integrity of the stored data. These tests prove that our SOG-LCD can work successfully without additional refresh operation frequently used in the conventional DRAM.

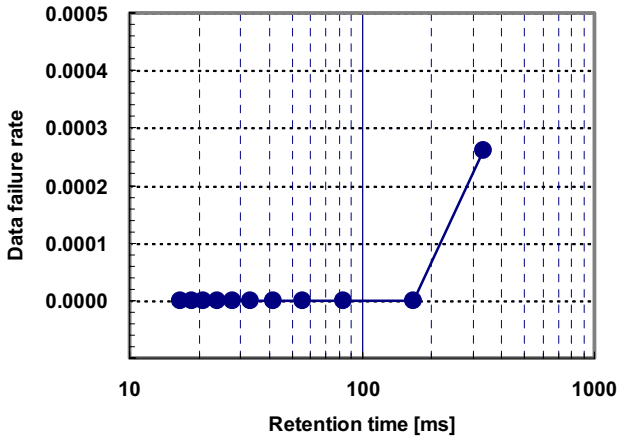

Fig. 6 Measured data failure rate vs. retention time in the embedded frame memory.

C. Example of display test

Figure 7 shows a photograph of our DRAM-embedded SOG-LCD under display test operation. The displayed data is input through the test circuit as the coded data. Clear stripes with regular pitch are shown and no defects were seen in this sample.

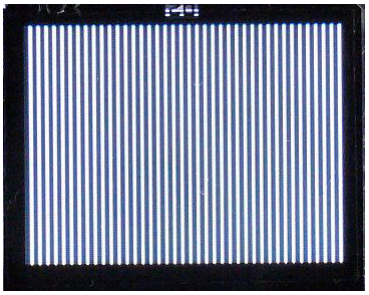

Fig. 7 Photograph of DRAM-embedded SOG-LCD under display test.

4. Summary

Quad-functional built-in test circuit has been developed for DRAM-frame-memory embedded SOG-LCD. Using the multiplexed input flip-flop as the circuit element, quad functionality, which consists of memory test, display test, serial data transfer test and parallel data transfer test, is realized. Measured examples of memory test operation show enough operation frequency and stored data integrity. This built-in circuit contributes to functional tests of embedded DRAM frame memory and the display picture-frame size reduction.

5. References

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