Nonvolatile memory devices with oxide-nitride-oxynitride stack structure for system on panel of mobile flat panel display

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Abstract

In this work, nonvolatile memory (NVM) devices for system on panel of flat panel display (FPD) were fabricated using low temperature polycrystalline silicon (LTPS) thin film transistor (TFT) technology with an oxide-nitride-oxynitride (ONOn) stack structure on glass. The results demonstrate that the NVM devices fabricated using the ONOn stack structure on glass have suitable switching characteristics for data storage with a low operating voltage, a threshold voltage window of more than 1.8 V between the programming and erasing (P/E) states after 10 years and its initial threshold voltage window (ΔV_{TH}) after 10^5 P/E cycles.

1. Introduction

For applications such as SOP, additional functional devices on glass have been fabricated. The study of FPDs made with NVM devices is an interesting research topic, because of their low-power consumption and use in panel control systems. Some groups[1-3] have carried out research on memory embedded in the pixels of FPDs, in order to reduce their power consumption. NVM devices are used to enhance the brightness of static images and reduce the power consumption, as in the case of the fabrication of direct memory in pixels (MIP) on glass panels. In the case where ELA is used, a high surface roughness is obtained due to the melting/crystallization of the substrate during the irradiation of the laser beam. In this work, instead of conventional CVD, plasma-assisted oxynitridation is utilized to form a uniform tunneling layer, because the planarization process is not suitable for the sequence of operations currently used in practical semiconductor processing. The characteristics of the LTPS NVM devices fabricated on glass in this study were investigated.

2. Experimental

Poly-Si film formed using ELA was used for the fabrication of the eFlash cells on glass. It was fabricated on a glass substrate by low temperature plasma processes. After the deposition of amorphous silicon (a-Si) film, the a-Si film was crystallized by excimer laser annealing (ELA). After the active region was patterned, The ONOn stack structure was formed with a thin tunneling oxynitride layer having a thickness of 2.3 nm, a charge trapping layer with a thickness of 20 nm, and a blocking oxide layer with a thickness of 12.5 nm. For the creation of the uniform tunneling layer, the rough poly-Si surface was exposed to N_2O plasma. After the deposition of SiO_2 as a blocking layer, aluminum was evaporated as a gate metal and the ion showering method was used to form p^+ doping in the source/drain regions, in view of the compatibility required during the fabrication of TFTs and eFlash cells for future real applications involving OLEDs. P-channel TFTs have generally been used for the driving part of OLEDs, because the source or drain region of the TFT which functions as the driving part is connected to the anode electrode of the OLED.

3. Results and discussion

The typical transfer characteristics of the LTPS NVM device due to programming and erasing are shown in Fig. 1. The NVM device was programmed and erased by applying gate biases of -9 V and +9 V for 1 ms to the control gate under V_S=V_D=0, respectively. The holes tunnel from the valence band of the poly-Si through the tunneling oxynitride film during the

programming operation, are trapped in the forbidden gap of the nitride layer and, consequently, the threshold voltage is shifted in the direction of negative voltage. The electrons tunnel from the poly-Si through the tunneling oxynitride film during the erasing operation, and either recombine with the holes trapped in the nitride layer or the trapped holes may be emitted from the trap state to the channel. The difference in the threshold voltage shift is large enough to define the "0" or "1" states for a logic memory circuit.

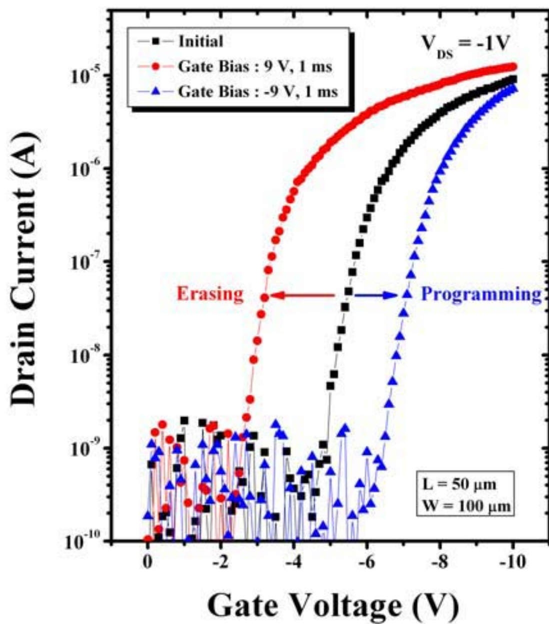

Fig. 1. Typical transfer characteristics of LTPS NVM with ONOn stack structure on glass. A gate bias of -9 V and a pulse width of 1 ms were used for programming and a gate bias of +9 V and a pulse width of 1 ms were used for erasing under V_S=V_D=0.

The retention characteristics of the LTPS NVM device on glass are shown in Fig. 2. For the programming and erasing operations, the LTPS NVM device on glass was biased under the conditions of V_G = -9 V and V_S = V_D = 0 for 1 ms and V_G = 9 V and V_S = V_D = 0 for 1 ms, respectively. The threshold voltage shifts were measured from 1 s up to 10^4 s. The difference in the threshold voltage between the programming and erasing states was initially 3.9 V and decreased to 3.25 V after 10^4 s. Though the NVM device was fabricated on rough poly-Si, the ΔV_{TH} was found to be more than 45% of the initial ΔV_{TH} after 10 years. The endurance characteristics of the LTPS NVM device with the MONOS stack structure on glass after P/E are shown in Fig. 3. The NVM device was programmed with a gate bias of -8 V and erased with a gate bias of +8 V for 1 ms under the condition, V_S=V_D=0. The initial ΔV_{TH} was retained after 10^5 cycles.

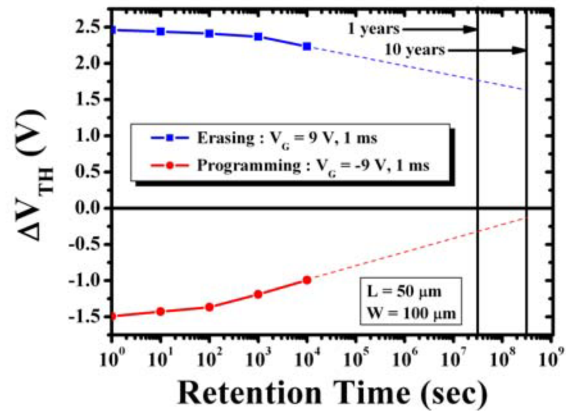

Fig. 2. Retention characteristics of LTPS NVM with ONOn stack structure on glass. The device was programmed and erased by applying -9 V and +9 V for 1ms to the control gate under V_S=V_D=0, respectively. The threshold voltage shifts are shown as a function of time.

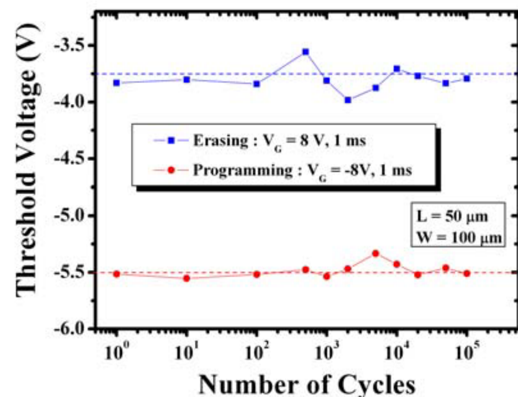

Fig. 3. Endurance characteristics of LTPS NVM with ONOn stack structure on glass. The device was programmed and erased by applying -9 V and +9 V for 1ms to the control gate under V_S=V_D=0, respectively.

4. Summary

This work reports the fabrication of p-channel LTPS NVM devices with an ONOn stack structure on poly-Si having a rough surface formed using ELA on glass, which are suitable for the real application of mobile FPDs as a solution to the problems related to the variation in the brightness of the panels following the change in the driving current. Because the fabrication of the NVM devices composed of an ONOn stack structure was carried out on poly-Si having a very rough surface, an ultra-thin oxynitride film was grown by the N_2O plasma-assisted process to allow for effective tunneling. The P/E operations can be achieved with a low operating voltage (< ±10V) applicable to mobile FPDs. The fabricated LTPS NVM devices on glass retained a ΔV_{TH} of more than 45% of the initial ΔV_{TH} after 10 years and its initial ΔV_{TH} after 10^5 P/E cycles. The LTPS NVM devices with the ONOn stack structure on glass reported in this work can be used in various kinds of display devices.

4. Acknoledgement

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