Drain induced barrier lowering and impact ionization effects in short channel polysilicon TFTs

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Keywords : polysilicon TFTs, short channel effects, drain induced barrier lowering

Abstract

The effect of channel length reduction on the electrical characteristics of self-aligned polysilicon TFTs has been investigated by combining experimental characteristics and 2-D numerical simulations. The role of drain induced barrier lowering and floating body effects has been carefully analized using numerical simulations.

1. Introduction

Future system-on-panel applications require a significant improvement in the performance of current polysilicon TFTs. The biggest leverage in circuit performance can be obtained by reducing channel length from the typical, current values of 3-6 μm to 1 μm, or less. Therefore, short channel effects in scaled down polysilicon TFTs will have to be controlled in order to allow proper operation of the devices. Recent works have shown several effects induced by channel length scaling, including parasitic resistance effects [1], kink effect enhancement [2] and threshold voltage (V_T) variation [3, 4]. Threshold voltage is known to be reduced in short channel MOSFETs by decreasing channel length and increasing source-drain voltage. This effect was explained by Troutman [5] by drain-induced barrier lowering (DIBL). However, in polysilicon TFTs, commonly fabricated on insulating substrates, floating body effects also represent another important factor influencing V_T. Indeed, when high electric fields are present at the drain end of the channel, impact ionization can be triggered and, similarly to SOI, the excess current is enhanced by the so-called parasitic bipolar transistor action [6]. The floating body effects have been shown to produce a severe degradation of the output characteristics in short channel TFTs, with an excess current scaling nearly as L^{-2} [2]. Therefore, in short channel polysilicon TFTs we can expect that both DIBL and floating body effects affect V_T. Understanding of the bias dependence of V_T is crucial in device and circuit designing.

In this work we have investigated the role of DIBL and floating body effect on the electrical characteristics of short channel polysilicon TFTs, with channel lengths down to 0.4 μm, by combining both experimental data and 2-D numerical simulations.

2. Experimental

Short channel (down to 0.4 μm) TFTs used in this work were fabricated at Philips Res. Lab, in Redhill, according to a process reported in Ref. [7] and adopting a self-aligned architecture. The polysilicon active layer, 40 nm thick, was formed by excimer laser crystallization. Source and drain contacts were formed by implanting P-ions through the gate oxide and doping activation was obtained by a second pass through excimer laser. The gate oxide was deposited in a PECVD system, using SiH_4 and N_2O gas mixture, to a thickness (t_{ox}) of 62 nm.

In Fig. 1 typical I_d-V_g characteristics, measured at V_{ds}=0.1 V and normalised at L=1 μm, are shown for different L. As can be seen from the linear plot (Fig. 1a), the effects of parasitic resistance are quite evident for L ≤ 2 μm while the subthreshold region (Fig. 1b) appears to be degraded only for the shortest L (0.4 μm). It should be noted that the off-current is L-independent at low V_{ds}, then, in the L-normalized plot, it increases with L. In Fig. 2a-b the variation of the transfer characteristics in the subthreshold region with V_{ds} are reported for two typical cases: short channel (L=0.4 μm) and long channel (L=20 μm) TFTs. From the data it appears evident that as L is reduced the spread in the transfer characteristics increases, denoting a substantial threshold voltage variation with

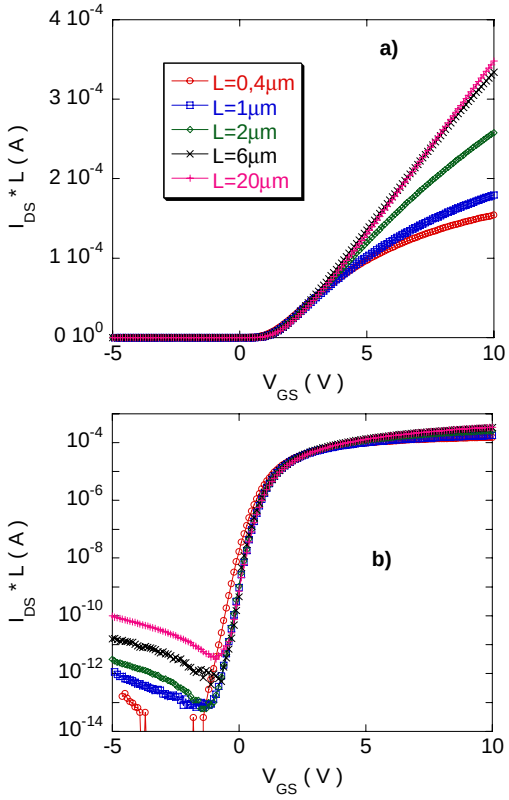

Fig. 1. Normalized transfer characteristics for different L in linear (a) and log (b) scales.

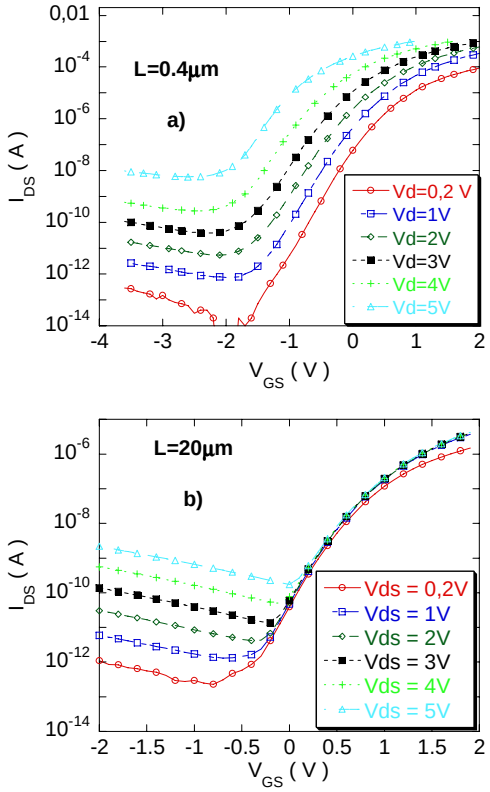

Fig. 2. Transfer characteristics for different V_{ds} and L=0.4 µm (a) and 20 µm (b).

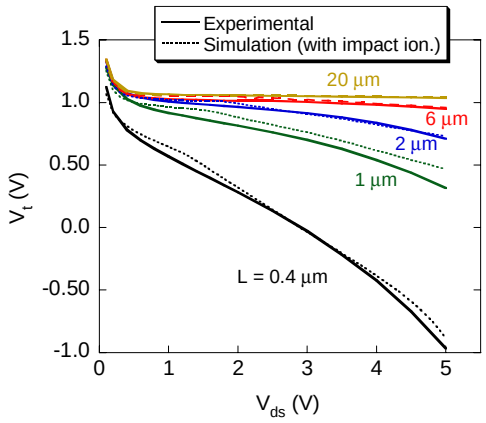

Fig. 3. Threshold voltage, V_T, vs V_{ds} for different L: experimental (solid lines) and simulated (dotted lines) data.

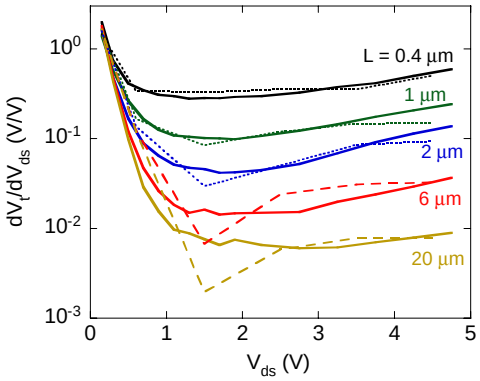

Fig. 4. Threshold voltage variation, $\delta V_T/\delta V_{ds}$, vs V_{ds} for different L: experimental (solid lines) and simulated (dashed lines) data.

V_{ds} in short channel TFTs. By defining V_T as the gate voltage at which I_{ds}= W/L 10^{-7} A, we determined the V_T values for devices with different L and in Fig. 3 the V_T dependence upon V_{ds} is shown. For short channel devices V_T is very sensitive to V_{ds} increase, while in long channel TFTs (L>2 µm) it is basically constant. From the data reported in Fig. 3 we determined the $\delta V_T/\delta V_{ds}$, a quantity which normally characterizes DIBL in MOSFETs [8], and in Fig. 4 it is shown for different L values. As expected, threshold voltage is much more sensitive to V_{ds} variations at short L, although the $\delta V_T/\delta V_{ds}$ curves, plotted on a logarithmic scale, show a similar trend for different L: after an initial decrease for V_{ds}<1V, there is a broad minimum, around 2 V, followed by an increase at high V_{ds}. In particular, we found a $\delta V_T/\delta V_{ds}$ value of 300 mV/V for L=0.4 µm at V_{ds}=2V, which then decreases nearly as L^{-1}, as shown in Fig. 5a. Also shown in Fig. 5b is the

$\delta V_T/\delta V_{ds}$ vs L plot at V_{ds}=4.5 V, showing the same L^{-1} trend. In addition, the output characteristics, measured in a TFT with L=0.4 μm in the subthreshold regime, show a strong V_{ds} dependence, as shown in Fig. 6, in contrast to long channel devices.

3. Numerical simulations

To clarify the role of impact ionization and DIBL on the V_T variation in short channel devices, we have simulated the electrical characteristics by the numerical programme DESSIS, adopting the effective medium approximation [1-3, 6]. By using a set of optimized parameters for the density of states (DOS) and adjusting the parameters for impact ionization as well as for the mechanisms determining the off-current (Poole-Frenkel, trap assisted tunnelling and band-to-band tunneling [9]), we could reproduce the device characteristics very accurately also in the case of short channel devices, as shown in Fig. 6. Using the same set of optimized parameters the device characteristics were computed for different L devices. Threshold voltage was then evaluated from the simulated characteristics, using the same criterion adopted for the experimental data. As can be seen in Fig. 3, the simulated data nicely reproduce the V_T dependence upon V_{ds} observed experimentally. The $\delta V_T/\delta V_{ds}$ curves were also evaluated from simulations and in Figs. 4 and 5 we can also see a very good agreement between experimental and simulated data.

In order to evaluate the role of the floating body effects on the V_T bias dependence, we simply re-computed the device characteristics by turning off the impact ionization. In Figs. 7 and 8 the simulated V_T and $\delta V_T/\delta V_{ds}$ are shown with and without including impact ionization in the simulations. As can be seen from Fig. 7, in short channel devices a large fraction of the V_T variation is due to floating body effects. It should be pointed out that the reduced V_T variation with L at higher V_{ds}, observed in SOI devices [10], is not present in polysilicon TFTs, as can be readily realized from Fig. 3. Indeed, as V_{ds} is increased the V_T curves tend to spread out, denoting an increased V_T roll-off with L.

Concerning the $\delta V_T/\delta V_{ds}$ curves shown in Fig. 8, we can clearly see that floating body effects strongly influence the high V_{ds} region. This can be better viewed referring to Figs. 5a and 5b, where the $\delta V_T/\delta V_{ds}$ values calculated with and without impact ionization at V_{ds}=2 V (Fig. 5a) and 4.5 V (Fig. 5b) are shown vs L. In addition, we also plotted in the same

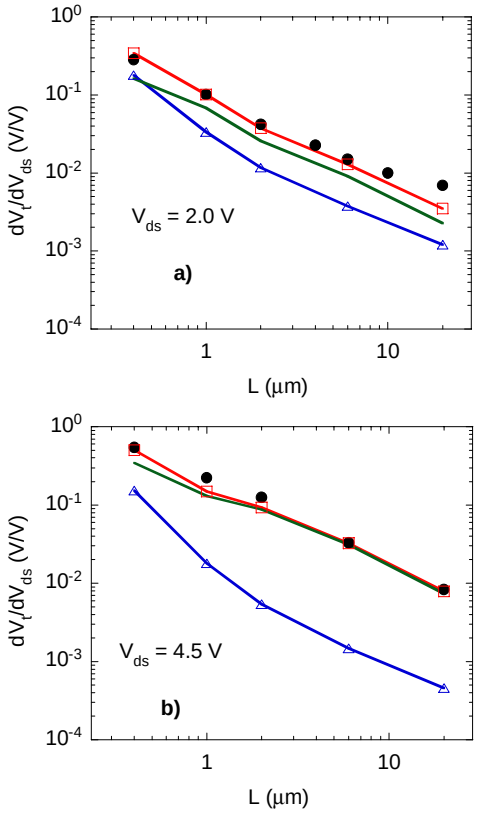

Fig. 5. Threshold voltage variation, $\delta V_T/\delta V_{ds}$, vs L for two different V_{ds}=2V (a) and 4.5 V (b): experimental data (●) and simulations with (red curves) and without (blue curves) impact ionization. Also shown is their difference (green curves).

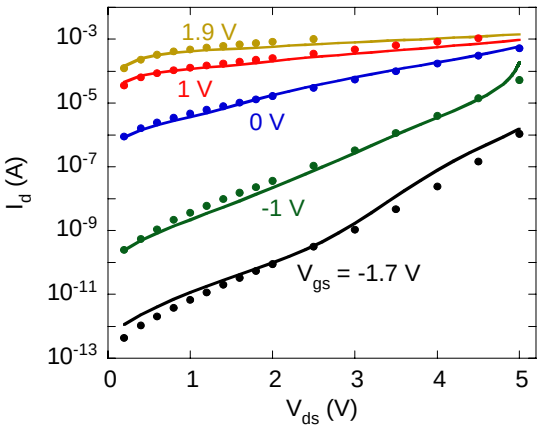

Fig. 6. Output characteristics measured at different V_{gs} in the subthreshold regime for a device with L=0.4 μm: experimental (●) and simulated (solid lines) data.

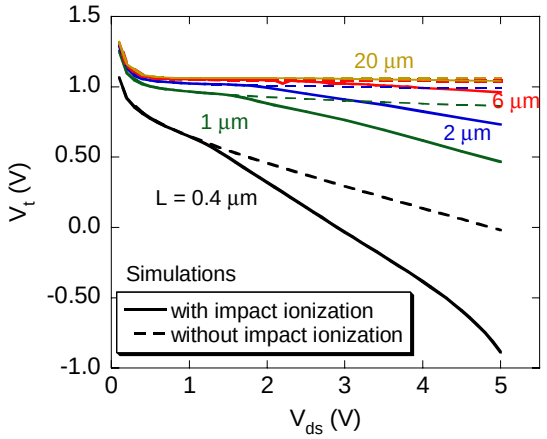

Fig. 7. Threshold voltage, V_T, vs V_{ds} for different L evaluated from simulations performed with (solid lines) and without impact ionization (dashed lines).

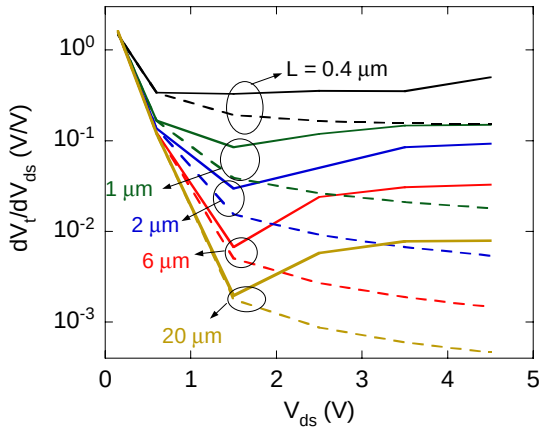

Fig. 8. Threshold voltage variation, $\delta V_T/\delta V_{ds}$, vs V_{ds} for different L, evaluated from simulations performed with (solid lines) and without impact ionization (dashed lines).

graphs their difference, which represents the contribution to $\delta V_T/\delta V_{ds}$ induced by the floating body effects. As can be seen, at V_{ds}=2 V the contribution induced by DIBL is already predominant at L=0.4 µm while at V_{ds}=4.5 V floating body effects are predominant, although DIBL already gives an appreciable contribution in short channel TFTs (about 1/3 of the $\delta V_T/\delta V_{ds}$ at L=0.4 µm). This is due to the fast rise at short L of the DIBL contribution and, by extrapolating the curves shown in Fig. 5b, it is reasonable to expect DIBL becoming the predominant mechanism controlling $\delta V_T/\delta V_{ds}$ also at high V_{ds} for L<0.25 µm.

4. Summary

Combining experimental data and numerical simulations we have analized the threshold voltage variation induced by drain bias in short channel polysilicon TFTs. Threshold voltage appears very sensitive to V_{ds} in short channel devices and the V_T roll-off with L tends to increase as V_{ds} is increased. According to numerical simulations performed with and without impact ionization, it appears that while DIBL is already controlling the device characteristics at low V_{ds} in L=0.4 µm devices, the shortest L used in this work, floating body effects predominate such variations at high V_{ds}. On the other hand, DIBL is expected to become predominant also at high V_{ds} for L<0.25 µm.

Acknowledgements

The authors wish to thank Dr. S.D. Brotherton for many useful discussions and for providing the devices.

5. References

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