SELAX Technology for Poly-Si TFTs Integrated with Amorphous-Si TFTs

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Keywords : A-LTPS, SELAX, Multi-offset TFT

Abstract

We developed the advanced LTPS (A-LTPS) manufacturing process. The a-Si TFT process was combined with selectively enlarging laser crystallization (SELAX) technology to improve the carrier mobility in the region where the peripheral circuits are to be fabricated. A 2.4-inch IPS-pro LCD panel for personal digital assistant use was successfully fabricated using the developed technology.

1. Introduction

In recent years, low temperature polycrystalline Si (LTPS) TFTs are widely adopted to realize LCD panels with high resolution for mobile displays such as for cellular-phones and for digital still cameras. This is because the LTPS TFTs has higher carrier mobility compared with the conventional amorphous Si (a-Si) TFTs. Therefore, LTPS panel enable the inclusion of peripheral circuits, and fewer connections. On the other hand, the manufacturing cost of a-Si TFTs is generally lower than that of LTPS TFTs. To achieve both of the high performance and the low cost panel, we developed the advanced-LTPS (A-LTPS) process. The only amorphous Si layer in the region where the peripheral circuits are to be fabricated is selectively converted to poly-Si. This enables us to fabricate LCD panels whose performance is identical to LTPS panel and whose fabrication process is almost compatible to that of a-Si TFTs panel.

In this paper, we will report the outline of the A-LTPS process and the decrease of the off-current which we used the multi-offset device structure. And we fabricated the prototype panel using the A-LTPS technology

2. SELAX Technology for A-LTPS

The SELAX technology is originally developed to enlarge the grain size of the poly-Si layer formed by excimer laser crystallization (ELC). The solid-state continuous wave (CW) laser beam (λ = 532nm) is scanned over the surface in one direction, and as lateral crystal growth occurs sequentially[1-2].

In the present work, to omit the ELC process for simplicity, an a-Si layer is directly irradiated by the CW laser. The schematic of the process and the

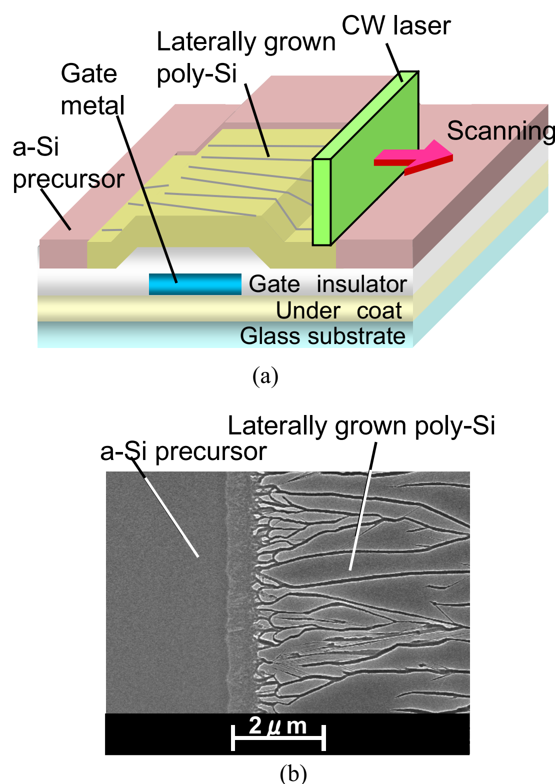


Figure.1 SELAX technology. (a)Schematic of the process, (b)SEM micro graph

scanning electron micrograph (SEM) of the irradiated sample after the secco etch to delineate the grain boundaries are shown in Fig. 1(a) and (b). There is a gate electrode under the a-Si precursor film because it is bottom gate structure. As can be seen from Fig. 1(b), lateral crystal growth starting from the amorphous precursor is clearly observed, verifying that the poly–Si layer can be obtained by using this process. Since the SELAX technology enable us to form poly-Si layer only in the region where the poly-Si is required and leave rest of the portion amorphous, the process is quite suitable to meet our end.

3. A-LTPS fabrication process

A schematic device structure of A-LTPS is shown in Fig. 2. The fabrication process is based on the a-Si TFT process so as to utilize a-Si TFT production line,

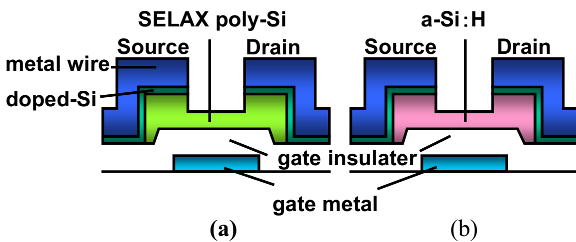


Figure.2 Cross sectional view of A-LTPS. (a)LTPS-TFT,and (b)a-Si TFT

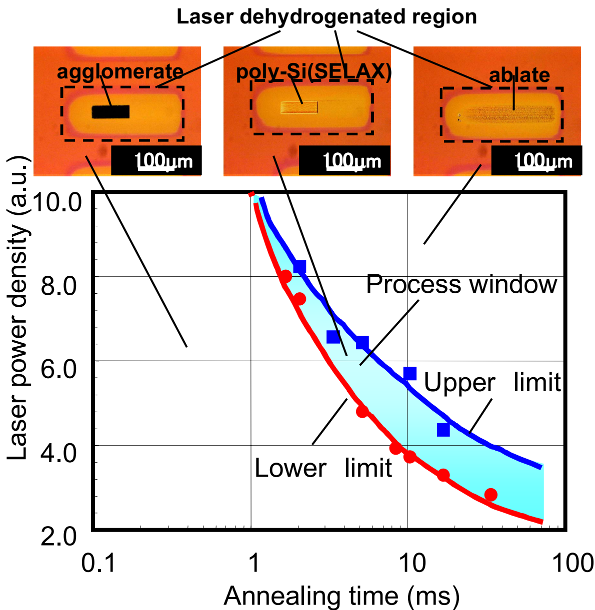


Figure.3 Process window of the laser dehydrogenation.

and the bottom gate structure TFT is adopted. Since this a-Si layer is used as the channel layer of a-Si TFT, it must be a hydrogenated a-Si layer. On the other hand, dehydrogenation of the a-Si is required to achieve laser crystallization. To solve this contradiction, we developed two optional processes. The first one is to partially dehydrogenate the a-Si layer that is to be polycrystallized by laser irradiation. The CW laser used for SELAX process is also utilized for laser dehydrogenation. The CW laser is selectively irradiated onto amorphous Si layer for dehydrogenation. Fig. 3 shows dehydrogenation process window, with laser power and laser irradiation period, and surface images of the dehydrogenated and SELAX processed poly-Si layer. The portion bordered by the upper limit curve and the lower limit curve depicts the condition required for obtaining dehydrogenated Si layer. The laser power density margin tends to increase with longer laser irradiation. The optimal annealing period for the process is determined as 10ms or more. Therefore, partial dehydrogenation is realized by using CW laser.

Since the processing time of the laser dehydrogenation process is long and results in poor throughput, another option is prepared. In the process, the a-Si layer goes through normal dehydrogenation process. After definition of the poly-Si layer, the a-Si:H layer, which is to be used for a-Si TFT, is deposited again by PECVD. The cross sectional structures of the devices are as shown in Fig. 4. By adopting this TFT structure, the ion implantation process conventionally used in the LTPS-TFT process to form source and drain region, and the dopant activation process are eliminated leading to fabrication cost reduction. The total process is basically the same as that of the standard amorphous TFT process, except for the additional process of crystallization using a CW laser.

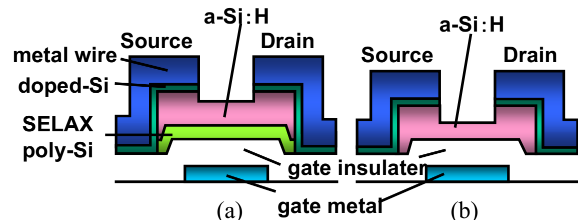
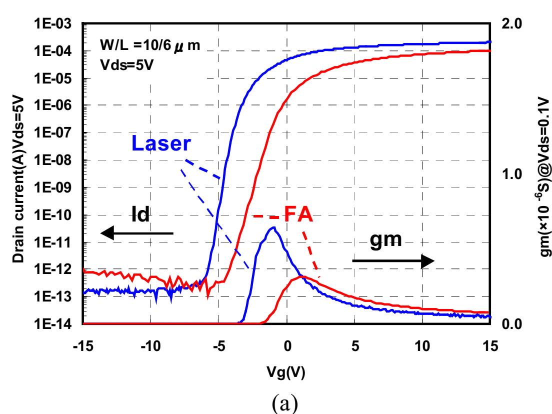


Figure.4 Cross sectional view of A-LTPS with a-Si/poly-Si double layers. (a)LTPS-TFT,and (b)a-Si TFT

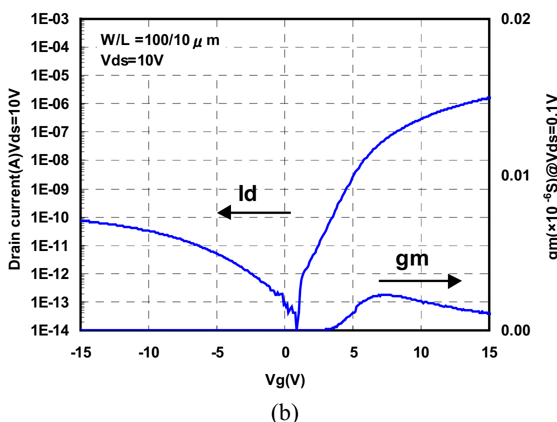
4. Experimental results

4.1 TFT characteristics of A-LTPS

The transfer characteristics (I_d-V_g characteristics) of a fabricated LTPS TFT and a-Si TFT are shown in Fig. 5(a) and (b) respectively. Fig. 5(a) shows two kinds of LTPS-TFT characteristics that each was adopted a different process. In Fig. 5(a), the graph titled "Laser" shows the LTPS-TFT which was fabricated by laser dehydrogenation process. The graph titled "FA" shows the LTPS-TFT which was fabricated by normal dehydrogenation process. The general characteristics are summarized in Table1. The characteristic of LTPS-TFT is improved compared with that of the a-Si TFT,



(a)



(b)

Figure.5 Tranfer characteristics (V_g-I_d,gm) of A-LTPS TFTs. (a)LTPS-TFT (b)a-Si TFT

Table.1 The general characteristics of A-LTPS. (a)LTPS-TFT and (b) a-Si TFT

	LTPS-TFT		a-Si TFT
	Laser	FA	
Vth(V)	-4.6	-3.2	5.1
S(V/decade)	0.3	0.6	1.2
Mobility(cm^2/Vs)	190	80	0.3

since the channel layer of LTPS TFT is made of laterally grown crystal. In LTPS -TFT characteristics, the threshold voltage (V_{th}), the subthreshold swing (S) and the field effect mobility are -4.6V, 0.3V/decade, and 190cm^2/Vs respectively. In addition, the characteristics of LTPS TFT fabricated by normal dehydrogenation process are -3.2V, 0.6V/decade, and 80cm^2/Vs respectively. The S increased and the field effect mobility decreased. The reason for this is the active layer has an a-Si layer which has a high resistance. However, from those results, it can be seen that a part of the peripheral circuit can be fabricated using these A-LTPS processes. Operation of gate voltage for demultiplexer is from 12V to -7V, thus the transistor whose V_{th} is about -5V, is applicable to LCD panel. This was done not to adopt ion implantation processes to adjust V_{th} for the simplicity of the fabrication process. The field effect mobility of LTPS TFT increased by order of more than 2 compared with that of the a-Si TFT. From these results, it can be seen that a part of the peripheral circuit is possible to be fabricated using the A-LTPS processes.

4.2 Off-current improvement for A-LTPS

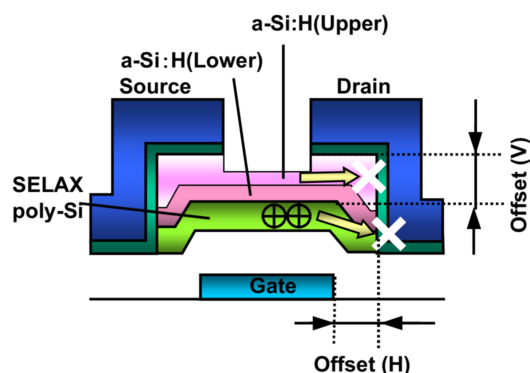


Figure.6 Cross sectional view of LTPS TFT. (Multi-offset TFT)

We examined a few types device structure to realize a low off current. Fig. 6 shows cross sectional view of the LTPS-TFT. To decrease off current, we adopted the structure that a-Si double layered and a potential barrier made by a doped Si., as shown in Fig. 6. A potential barrier by doped-Si controls the drift of electrons. A doped-Si layer formed to all under metal wiring and covering the top surface and side wall of the active region. An a-Si:H layer that is to be used for a-Si TFT adopted double layer structure. The field

effect of the gate electrode is low in the upper layer in comparison to the lower film. Therefore, the upper side of a-Si:H consists of a low conductive layer.

Furthermore, we developed the Multi-offset TFT to decrease drain field. If a gate electrode overlapped drain electrode, drain field increased, and off current increased. Therefore gate electrode and drain electrode adopted to offset structure (Horizontal offset). An a-Si:H layer on a poly-Si layer effected to decrease drain field (Vertical-offset). Fig. 7 shows each transfer characteristics of TFTs structures. The TFT performance adopted by the multi-offset structure is low off-current. When a gate overlapped a drain, or vertical offset is insufficient, off-current is increased. Thus the low off-current is realized by the decrease of drain field with the Multi-offset TFT.

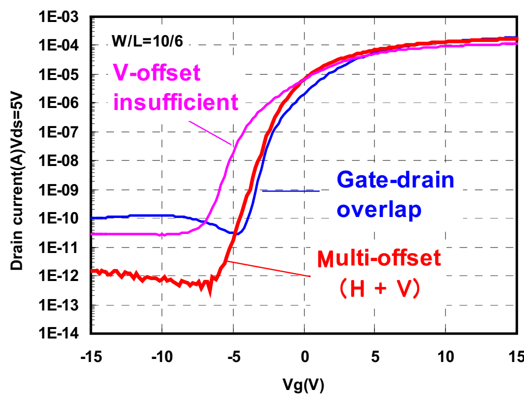


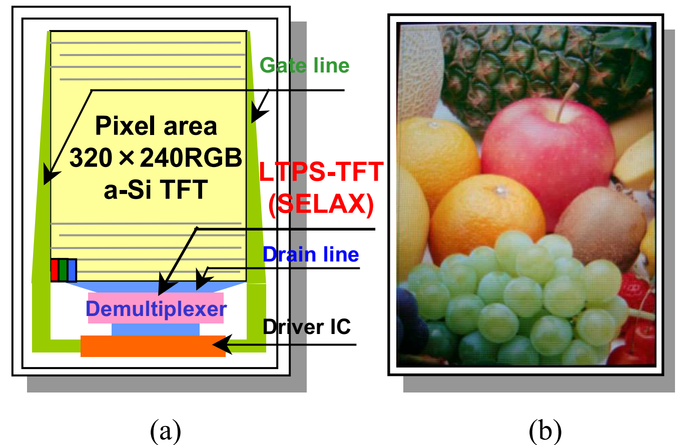
Figure.7 Transfer characteristics of the Multi-offset TFT, the Gate-drain overlapped TFT and V-offset insufficient TFT .

4.3 2.4-inch IPS-pro LCD panel

A 2.4-inch IPS-pro LCD prototype QVGA (320 x 240 x RGB) panel is fabricated using the A-LTPS process. The specification of the panel and the sample image are shown in Fig. 8. The pixel array consists of a-Si TFTs and the demultiplexer consists of A-LTPS TFTs. Since demultiplexer is fabricated on the panel, the number of signal wiring is reduced to almost 1/3 compared with the conventional a-Si TFT panel. Reduction of the number of wiring realized slim bezel LCD-display. We developed a driver IC for an A-LTPS panel. As a result, it was realized that the A-LTPS LCD panel was driven by one driver.

5. Conclusion

The A-LTPS manufacturing process, which enables production of LTPS-TFTs by utilizing the conventional a-Si TFT production line, is developed. By utilizing the SELAX technology, the fabrication of LTPS-TFTs integrated with a-Si TFTs is realized. We improved the device structure of the bottom gate LTPS-TFTs, and off-current was reduced. Since the panel with performance comparable to that of LTPS-TFT panel can be fabricated, the panel with high resolution such as VGA, can be produced with the conventional a-Si TFT production line. Moreover, the amount of capital investment is reducible in making a new production line compared with the conventional LTPS-TFT line.



(a) (b)

Figure.8 IPS-pro LCD QVGA panel. (a)Architecture, and (b)Sample picture of a 2.4-inch diagonal QVGA Display.

6. Acknowledgements

The authors would like to thank M. Ohkura and H. Shinmoto for their important discussions throughout this work. Thanks also extended M. Hongo, A. Yazaki and all members of the Small and Medium Product Technology Department, Hitachi Displays, Ltd., for their help in a trial production of the A-LTPS technology.

7. References

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