Improvement of Slit Photolithography Process Reliability for Four-Mask Fabrication process in TFT LCDs

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Keywords: four mask process, Slit mask process

Abstract

In order to reduce the manufacturing cost of TFT LCDs and cut down an amount facilities invested, there are many LCD panel makers contributes to convert the current Five-mask manufacturing process into the noble Four-mask fabrication process. We optimized the slit mask to improve the poor process reliability.

1. Introduction

Currently many companies in the LCD industry have been using the four-mask technology [1] as a standard process to reduce the process steps and the manufacturing cost. Until now, it is the most effective technology for four-mask technology to maximize the investment efficiency and to minimize the manufacturing cost in the LCD fabrication process. When a TFT LCD array fabrication factory which designed a current five-mask fabrication process is changed into a noble four-mask fabrication process, the rate of increase of the total production can be maximum 25%. As for the core technologies to realize a four-mask fabrication process, one is the slit photolithography mask technology [2], which is used the slit mask which is designed for the double slit shape, and the other is the multilayer etching technology with a continuous dry etch process in the one chamber to make up for a current four-mask's shortcoming[3,4]. It is necessary for slit mask to form the partially exposed photoresist which protect the amorphous silicon layer of a channel region during a source drain metal and an active layer is etched. But the slit photolithography process can cause many kinds of troubles because it is very sensitive to the process variation. So many companies are focusing on the improvement of production yield of a four-mask fabrication process. Some companies successfully apply the new fabrication process for mass production. But some of companies have been developing the optimized process and design to solve the defects which caused by four-mask fabrication process. [5]

Main processes of yield loss in four-mask fabrication process are a photolithography process and a source-drain multiple etching process for formation of TFT channel.

In this article, we introduce about the cause of production yield loss, and we propose their solution to improve these problems.

2. Experimental

We use a process, which is source-drain etching process composed by Active etch, P.R etch back, channel Mo etch, back channel is completely continuous one chamber dry etching process for the stable TFT channel formation.

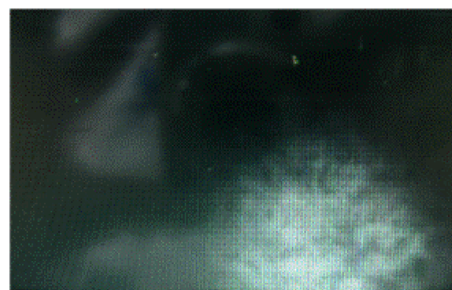

Figure 1 Phenomenon of Mura in abnormal panel

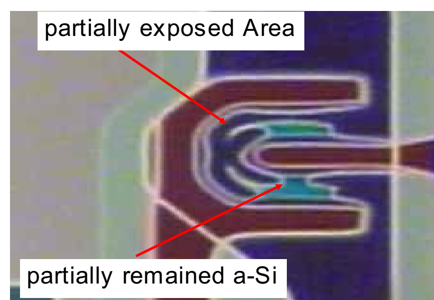

Figure 2 partially removed amorphous silicon in the channel area

Figure 1 shows main defect which occurred in cell process when we produce the panels to use the four-mask fabrication process. The white area is the abnormal area that happens to the Mura.

Figure 2 shows a picture of channel region which removed part of amorphous silicon at white Mura area of Figure 1. Such thin film transistor couldn't operate normally. Partially removed amorphous silicon can cause the pixel defects and the Mura defects, which occur at low thickness region of partially exposed photoresist.

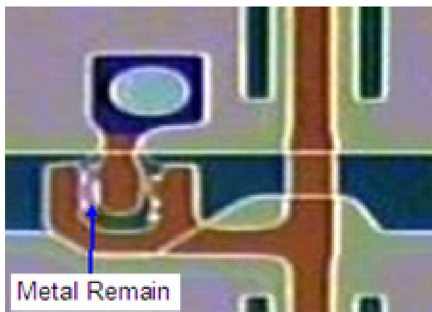

Figure 3 Pixel Shape of Short circuit

Figure 3 shows a short circuit defect, which is occurred when the source drain metal don't removed. These kinds of defects caused by bad uniformity of partially exposed photoresist at the slit photolithography process. The yield loss at four-mask fabrication process depended on defects which caused by bad uniformity of thickness of partially exposed photoresist at slit photolithography process.

4. Result and Discussion

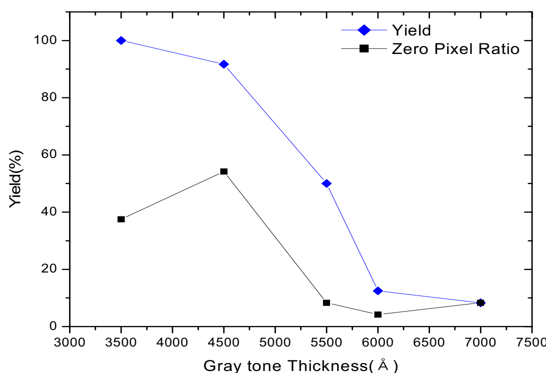

Fig.4 Current production yield at 4mask process

Figure 4 shows the production yield and the percentage of zero pixel panels according to the change of thickness of partially exposed photoresist at the four-mask fabrication process. The cause which decreased the production yield at partially exposed photoresist below 4000Å resulted from increasing the pixel defects by the removed amorphous silicon such as Figure 2. In case the thickness of photoresist is low, source drain metal can be removed by source drain etchant at the source drain wet etch process because the photoresist didn't cover the source drain metal of channel region at some position. In the next step, the amorphous silicon which can not be cover by the metal at channel region is removed by SF6-Cl2 gas mixture at active etch step of the source drain multiple etch process. At the partially exposed photoresist over 4500 Å, the percentage of zero pixel panels decreased rapidly and production yield decrease also. It is caused by the increase of short circuit defects in the channel such as Figure 3. It means that partially exposed photoresist can not be ashed clearly during the photoresist etch back step of source drain multiple etch process because photo resist is too high at its bad uniformity region. So Mo metal can not be removed entirely because the photo resist which don't removed in the channel area is prevent the source drain metal etch. Consequently, the change of production yield is subject to thickness change and uniformity of partially exposed photoresist at the four mask fabrication process.

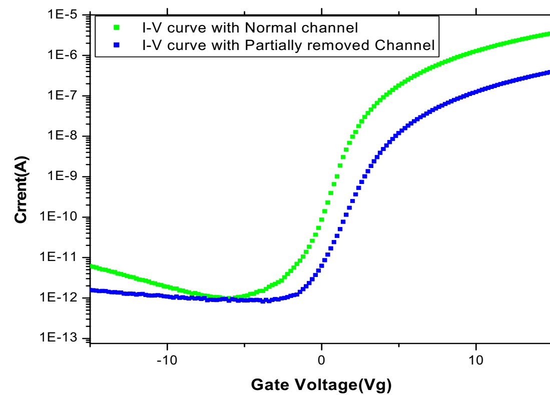

Fig. 5 comparison of Transfer curve

Figure 5 shows I-V characteristics of TFT channel with the amorphous silicon in normal area and with partially removed amorphous silicon in mura area such as Figure 1. TFT Ion characteristic of channel with partially removed amorphous silicon is lower than Ion current with normal channel. The W/L of channel with partially removed

amorphous silicon become small, so Ion characteristic is lower than normal channel. In order to charge the pixel, Ion current must be high sufficiently. Generally, charging ratio must satisfied approximately 99% and over. So, Ion current of channel with partially removed amorphous silicon couldn't charge a pixel charge sufficiently, quality of display become poor by brightness difference.

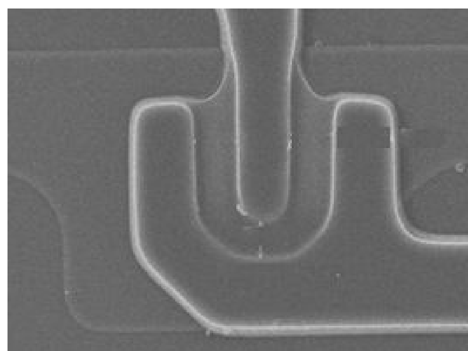

Figure 7 Top view of Channel area

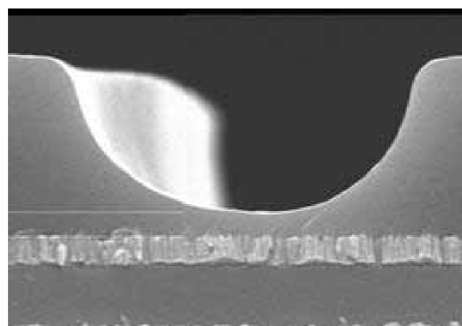

Figure 8 Sectional View of Channel area

Figure 7 shows a top viewed SEM when thickness of partially exposed photoresist is 3000Å. Figure 8 shows a cross-sectional viewed SEM of channel in Figure 7. Distance between tops of the photoresist is approximately 3.8 ㎛. Channel length at the 1 ㎛ from bottom of photoresist is approximately 2.8 ㎛, and the channel length between a source and a drain after the source drain multiple etch is 3.8 ㎛ below. Generally the patterning resolution of a exposure machine can not guarantee to pattern the resolution below 4 ㎛ at the TFT LCD. Therefore, if channel length of the partially exposed region at the 1 ㎛ position from bottom of photoresist is 4 ㎛ and below, the channel length and partially exposed thickness has a poor uniformity as equipment condition.

Its poor uniformity took place because the exposure energy through slit mask with narrow channel changed as equipment condition. So the short circuit defects occur regardless of the thickness of partially exposed photoresist in the narrow slit design.

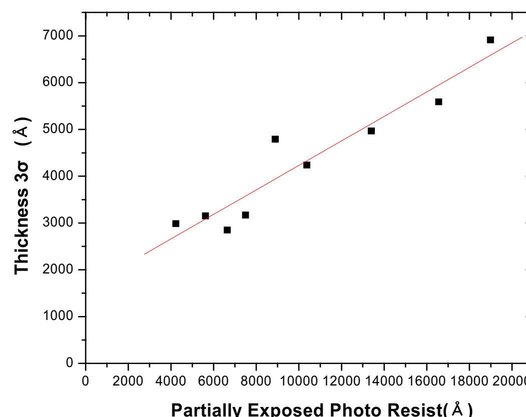

Figure 9 Thickness 3σ of partially exposed photoresist

Figure 9 shows 3σ of the photoresist thickness according to the changes of the partially exposed photoresist in the glass. At the high thickness region of the partially exposed photoresist, the thickness of partially exposed photoresist is difficult to control accurately because the thickness variation is big according to the glass position. Consequently, the array yield decreased suddenly by increasing of the short circuit defects.

Figure 10 shows the each variation of the measured channel length after the source drain multiple etch process according to the thickness changes of partially exposed photoresist.

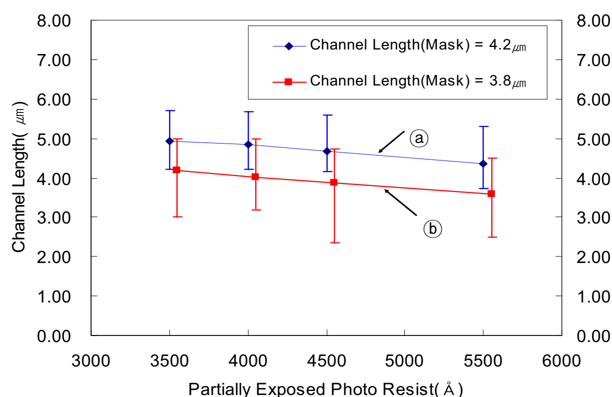

Figure 10 Comparison of channel length as Masks

Plot ⓑ is the variation of channel length in the glass when the channel length of slit mask is 3.8 ㎛, and Plot ⓐ is the variation of channel length in the glass when the channel length of slit mask is 4.2 ㎛. The variation of channel length of plot ⓑ is bigger than the variation of channel length of plot ⓐ in the same thickness of partially exposed photoresist. It is found that slit parameters have influence on channel length and its variation. At the four-mask fabrication process, The maximum difference of variation of channel length between plot ⓐ and ⓑ is approximately 0.5 ㎛. If their difference 0.5 ㎛ is converted into thickness of photo resist, the converted PR thickness is approximately 2000Å. Therefore, when the slit design of plot ⓑ applied, the photolithography process has a poor process reliability.

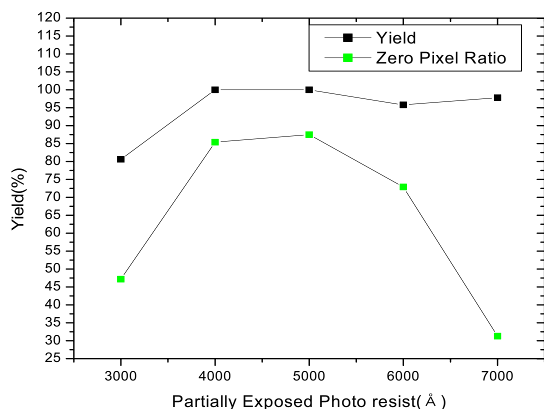

Figure 11 Improved Production yield at 4Mask process

Figure 11 shows a yield when we use the slit design of the plot ⓐ in Figure 10. Compared with Figure 4. which uses slit mask of 3.8 ㎛, the panels ratio without pixel defects is more high, and the production yield is more stable at partially exposed photoresist 4000Å and over. The mura and pixel defect by partially removed amorphous silicon occurs at the thickness of photoresist 4000Å below, and the short circuit defects by partially remained metal begins to occur from the thickness of photo resist 5000Å over. According to the production yield of Figure 11, the slit design with wide channel length is better to improvement of productivity because the photolithography process reliability is good and the production yield is high.

6. Conclusion

In order to improve the production yield in the four-mask fabrication process, many TFT LCD companies have endeavored to improve the process reliability for many years.

We accomplished reliability of slit photolithography process by optimization of slit mask design. We prove that the thickness variation of photoresist depends on the slit parameters and the channel length size. As a result, the slit photolithography process is required to optimize not only the photolithography process but also the slit mask design. After all, the improvement of slit photo process reliability by optimization of the slit design parameters make possible to obtain the high production yield.

7. Acknowledgment

The authors would like to appreciate the engineers of four-mask process project.

8. Reference

[1] C.W. Han, “A TFT Manufactured by 4Masks Process with photolithography” *Asia Display 1998,* p.1109 (1998)

[2] Jean H. Song, D.J. Kwon, S.G. Kim, “Advanced Four-Mask process Architecture for the a-Si.” *SID 2002 Digest*, p1038 (2002)

[3] Z.T. Wang, T.Y. Min, H.J. Qiu,” Investigation on Metal RIE Dry Etching conditions in the Thin Film Transistor 4Mask Fabrication Process" *Asia Display 2007*, p1219 (2007)

[4] H.J Qiu, Z.T. Wang, T.Y. Min, W.B. Gao, S.U. Choi "Oxygen and Sulfur Hexafluoride Added Plasma Ash in Reactive Ion Etch on channel region in TFT Array Process" *IDW 2007 Digest*, p546 (2007)

[5] T.Y. Min, Z.T. Wang, H.J. Qiu, W.B Gao, S.U. Choi, S.K. Lee “Investigation on the causes that affected the Channel Length in the 4Mask Fabrication Process” *IDW 2007 Digest*, p. 1959(2007)