10-bit Source Driver with Resistor-Resistor-String Digital to Analog Converter Using Low Temperature Poly-Si TFTs

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Abstract

A 10-bit source driver using low temperature poly-silicon(LTPS) TFTs is developed. To reduce the DAC area, the DAC structure including two 5-bit resistor-string DACs and analog buffer, which has analog adder is proposed. The source driver is fabricated using LTPS process and its one channel area is 3,200μm × 260μm. The simulated INL and DNL of output voltages are less than 3 LSB and 1 LSB, respectively.

1. Introduction

Recently, the integration level of low-temperature-poly-silicon (LTPS) TFT-LCD has been increasing. There are several researches of integrating gate driver, de-multiplex switches, DC-DC converter and source driver using LTPS TFTs [1-3]. However, the integration of source driver is getting harder because the source driver circuits require a high accuracy analog buffer and a compact digital-to-analog converter (DAC).

There are two issues for design of source driver using LTPS TFTs. Firstly, the DAC should be designed area-efficiently because the area of the source driver depends on that of DAC in source driver. In the conventional 6-bit source driver which adopts decoder-based resistor-string DAC, the DAC occupies about 60% of the whole area of source driver. Since the area of the decoder-based resistor-string DAC doubles with every one bit increase in data, the area of 8-bit DAC takes four times as large as that of 6-bit DAC. To implement an 8-bit DAC with the decoder-based resistor-string type is impractical. To make the area of source driver small for cost effectiveness, it is highly required to reduce the area of the DAC [4].

Secondly, the source driver must control its output voltage accurately within intervals of around 5 mV at 8-bit resolution. Therefore, accurate DAC and analog buffers are required. Moreover, because one source driver has several hundreds of analog buffers and each analog buffer has its own offset voltage which comes from the process variations, the channel-to-channel offset variations as well as the absolute offset voltage of its own should be reduced.

To solve these problems, we proposed the area-efficient resistor-resistor-string DAC and the analog buffer with an analog voltage adder.

2. Proposed driving method

Fig. 1 shows the block diagram of the proposed DAC and analog buffer. It consists of two 5-bit resistor-strings, two switch arrays, two 5-bit decoders and an analog buffer. The 1st R-string divides GMA1 to GMA2 into 32 levels (VC0~VC31), where GMA1 is 5V and GMA2 is 2V. V_{COARSE} is selected among these voltages by 5-bit decoder and connected to the analog buffer. The 2nd R-string divides GMA3 to GMA4 into 32 levels (VF0~VF31), where GMA3 is 100mV and GMA4 is 0V. V_{FINE} is selected among these voltages by 5-bit decoder and connected to analog buffer. The analog buffer output is sum of V_{COARSE} and V_{FINE}. Thus, the proposed structure can represent 10-bit gray scale.

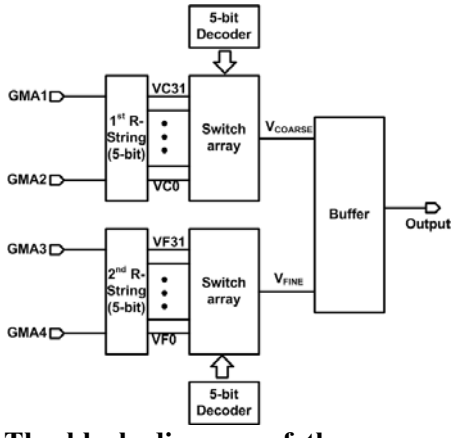


Fig. 1. The block diagram of the proposed DAC and analog buffer.

To use an analog buffer for summation of V_{COARSE} and V_{FINE}, a previously reported analog buffer for LTPS TFT is modified. Generally, conventional analog buffers are composed of a differential amplifier. However, because LTPS TFT has inferior electrical characteristics such as high threshold voltage and non-uniformity of electrical properties, there are many problems to design the accurate analog buffer. To overcome these problems, there have been a lot of researches. The analog buffers such as comparator type [1], source follower type [4], and common source type [5] have been developed. The developed analog buffers in Fig. 2 have feedback system using capacitor.

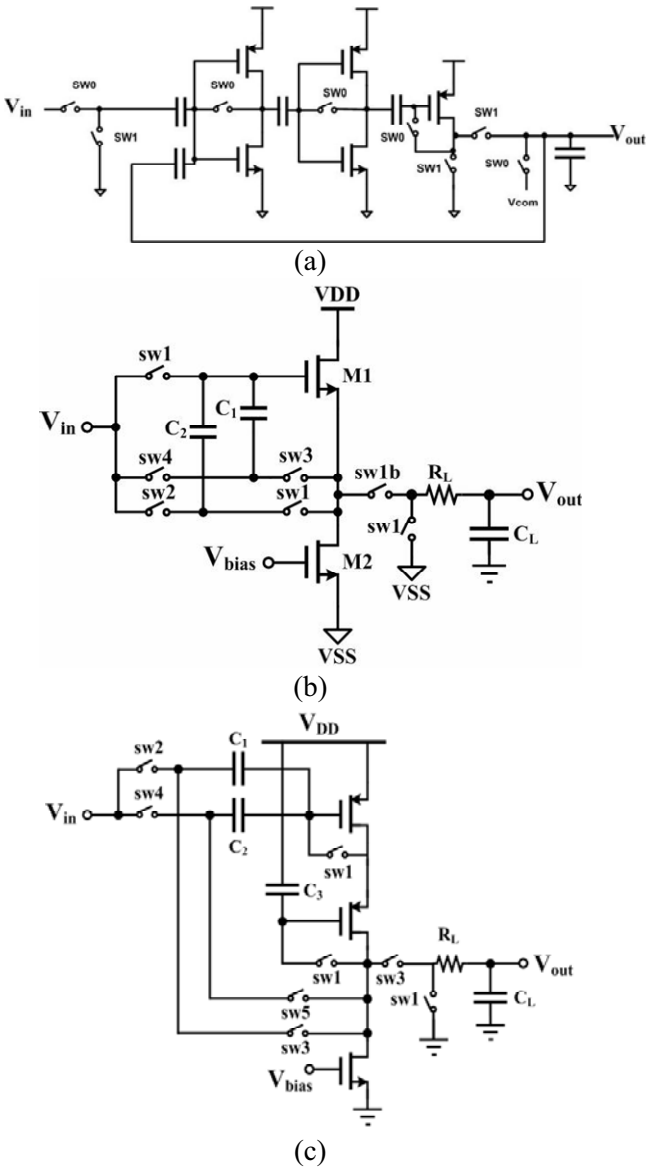


Fig. 2. Schematic diagrams of the previously reported analog buffers. (a) comparator type, (b) source follower type, and (c) common source type.

In the proposed analog buffer, the feedback system is used for summation of V_{COARSE} and V_{FINE} by modifying previously reported analog buffer [5]. Fig. 3 shows the schematic diagram of the proposed analog buffer. In the proposed analog buffer, the capacitor (C_4) is added to the previously reported one [5] for analog voltage adder. The analog buffer has output with two feedback processes and V_{FINE} is added to output using capacitor (C_4) in the 2nd feedback process.

The proposed buffer operates in three phases: one sampling mode and two negative feedback modes. In sampling mode, SW1, SW4 and SW2 are on. Then, SW1 and SW2 are off at the end of sampling phase. Thus, the gate voltage of M1 is |VDD – Vth|. The voltage across capacitor (C_1) and capacitor (C_2) is Vin-|VDD - Vth|. And the gate voltage of M2 that is self bias |VDD – 2Vth| is stored to capacitor (C_3). In first feedback mode, SW3 is on. As soon as SW3 is on, the gate voltage of M1 becomes GND due to the capacitive coupling. The circuit operates the first negative feed back mode until output voltage equals to input voltage. To increase accuracy of output voltage, the circuit operates the second negative feed back mode, while SW5 is changed to turn on and SW3 is remains on. At this time, the resistance of M2 becomes high during negative feedback and the voltage of V_{FINE} stored in capacitor (C_4) is connected to the gate of M1. Then, the output voltage increases by V_{FINE}.

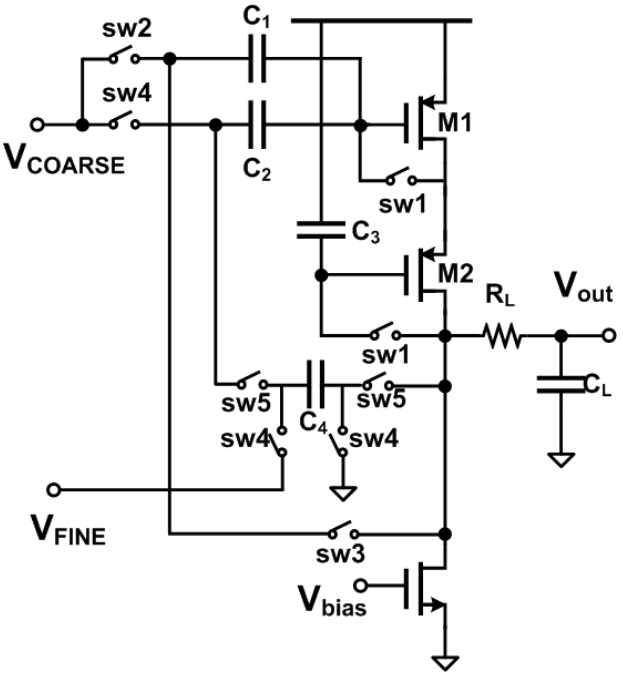


Fig. 3. Schematic diagram of the proposed analog buffer.

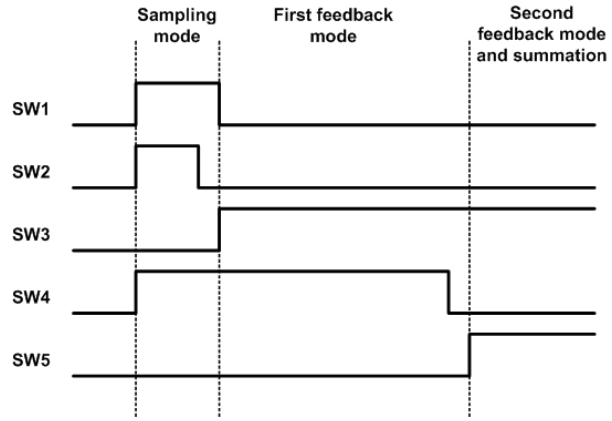
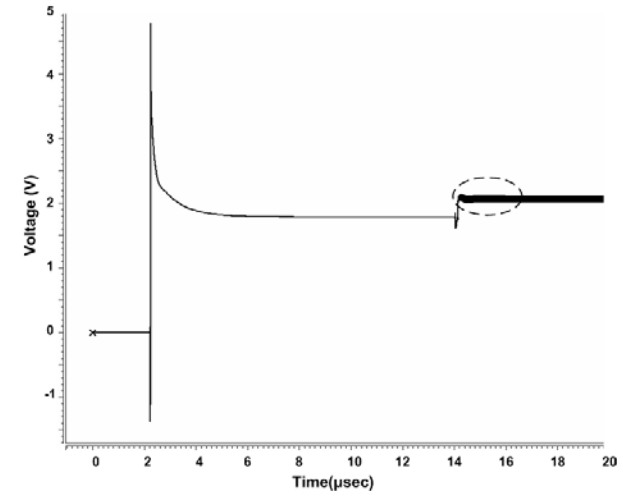
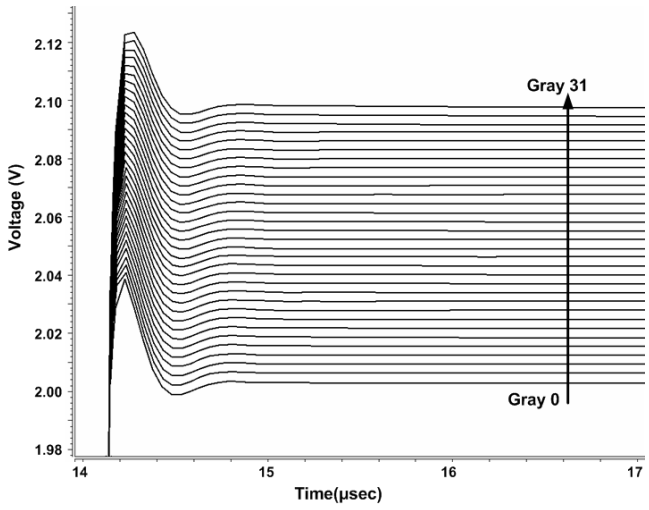


Fig. 4. The timing diagrams of the analog buffer.



(a)



(b)

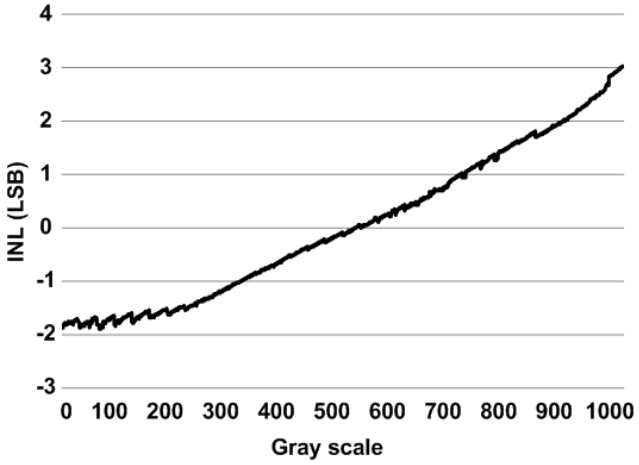
Fig. 5. The simulation results of output voltages. (a) output voltages between gray 0 and gray 31 and (b) magnification of circle in Fig. 5(a).

3. Simulation results

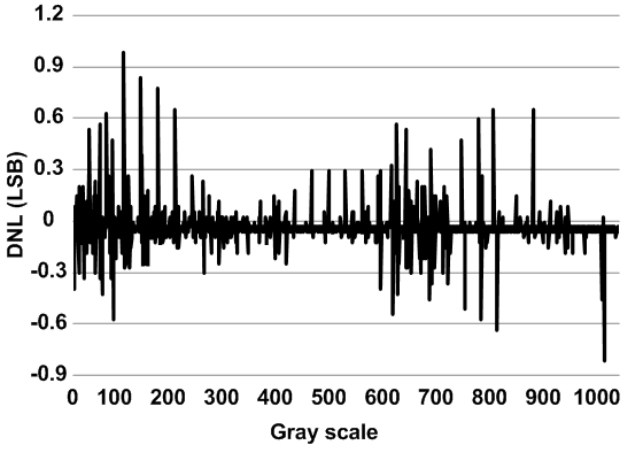
Fig. 5(a) and 5(b) show the simulation results of the output voltage waveforms between gray 0 and 31 and the magnification of circle in Fig. 5(a), respectively. As shown in Fig. 5, output voltage results in the sum of V_{COARSE} and V_{FINE}. The difference voltage of 1 LSB gray level is 3mV. As a result, the output buffer works as an adder of V_{COARSE} and V_{FINE}.

Fig. 6 shows the integral nonlinearity (INL) and the differential nonlinearity (DNL). The maximum errors of INL and DNL are less than 3 LSB and 1 LSB (3 mV), respectively.

Fig. 7 shows the micrograph of the fabricated source driver. There are two 5-bit resistor-string, switch array, 5-bit decoder and analog buffer. The chip is fabricated in the LTPS process and its one channel area is 3,200μm × 260μm.



(a)



(b)

Fig. 6. Simulation results of the proposed source driver. (a) INL and (b) DNL.

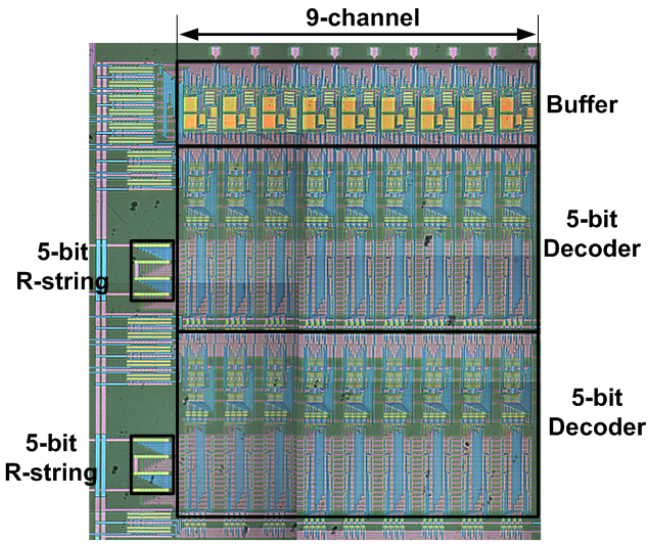


Fig. 7. The micrograph of the fabricated source driver.

4. Conclusions

We proposed a new source driver for 10-bit gray scale using LTPS TFTs. The proposed source driver is fabricated in the LTPS process and has 9 output channels. The developed driver consists of two 5-bit resistor-string DACs, and an analog buffer which has an analog voltage adder function. The area of the proposed DAC takes only 1.5 times as large as that of 6-bit decoder-based resistor-string DAC. The one channel area of fabricated driver is 3,200μm × 260μm. The simulated INL and DNL of output voltages are less than 4 LSB and 1 LSB, respectively. Therefore, the propose DAC structure can be a candidate for the integration of source driver using LTPS TFT.

5. Acknowledgements

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6. References

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